FINAL REPORT

DESIGN, DEVELOPMENT, FABRICATION AND DELIVERY OF IMPROVED MOS TRANSISTORS

Earl S. Schlegel

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National Aeronautics and Space Administration
George C. Marshall Space Flight Center
Huntsville, Alabama

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Period Covered: 21 May 1965 to 21 May 1966
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FOREWORD

This report was prepared by the Lansdale Division of the Philco Corporation, a subsidiary of the Ford Motor Company, under Contract No. NAS8-11926. It is the final report, covering studies performed during the contract period from May 21, 1965 to May 21, 1966.

The subject program was administered under the direction of Dr. A. M. Holladay of the Astrionics Laboratory, George C. Marshall Space Flight Center, Huntsville, Alabama. The program bears the Philco Corporation, Lansdale Division, internal number R-505.

ABSTRACT

MOS transistors are well suited for complex high density circuitry in electronic systems for space applications. In this program the causes of instability, high threshold voltage, and sensitivity to gamma radiation in MOS transistors were studied in detail.

Phase I called for a critical review of the published information to provide a firm basis for the program. Surveillance of the literature continued throughout the program.

Phase II called for the determination by radiochemical means of the exact species of charge responsible for the instability and high threshold voltage. The behavior of sodium as a cause of instability became evident from the literature. Our work showed that tritium introduced into the oxide in the form of tritiated water did not move in an applied field at elevated temperatures.

Phase III called for the development of techniques for removing mobile ions from the oxide to create stable devices. Our efforts to drift ions to the oxide surface and etch them away only partially reduced the mobile ion content of the oxides. Therefore, alternative techniques were sought and methods developed for minimizing oxide contamination to produce stable oxides having mobile ion densities below 5×10^{10} cm^{-2}. Investigations were made to determine the sources of various types of instability. These showed that alkali ion instability can be due to the water used in a wet oxidation, the metalizer, or the etching or rinsing solutions used before metalization of the oxide. A second type of instability, observable at room temperature, was found to depend upon the rinsing or etching of the oxide before the metalization and upon the heat treatment of the metalized oxide. A third type of instability, due to trapping, was found to be more pronounced in vapor plated oxides than in thermally grown oxides, and its magnitude depends on the silicon surface treatment before the oxide deposition. On the basis of this work, we now believe it possible to devise control procedures for preventing unstable devices from being used in space applications.

Phase IV called for the development of techniques to improve the electrical performance of MOS devices by neutralizing or removing immobile charge from the oxide to achieve lower transistor threshold voltages. Reducing the positive charge in the oxide makes it possible to operate transistors at lower power levels and to design transistors that are less likely to fail due to shorts through the oxide. Experimental techniques which lowered immobile charge densities include the use of different silicon orientations, the use of vapor plated rather than thermally grown oxides, thermally growing the oxide at a lower temperature, heat treating at 300°C, or nickel plating the underside of the wafer followed by a high temperature bake.

The advantages of MOS devices can be most fully utilized in space applications when means are found for improving their resistance to radiation in non-optimum space environments. Phase V called for the evaluation of each oxide for radiation resistance. The radiation resistance was found to be independent of whether the oxide was thermally grown or vapor plated, and independent of the silicon orientation, the mobile ion content, the irradiation temperature, and the silicon conductivity type. Better radiation resistance was found in a group of transistors which were made with a process involving a phosphorus deposition, a heat treatment and subsequent partial layer removal. Improved radiation resistance was also found in capacitors made with an oxide that was thermally grown at a lower temperature, and in a group of transistors made by another manufacturer. Some of the behavior of MOS devices in radiation can be explained by a physical model which will serve as a basis for further research efforts to improve the radiation resistance of MOS devices.

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1. INTRODUCTION

1.1 General

Integrated circuits are being designed for an ever-increasing variety of electronic equipment. The growing acceptance of integrated circuits is due to their low operating power levels, high reliability, low cost, small size, and light weight. This combination of features is well suited to the requirements of complex, high density circuitry in electronic systems for space applications.

Discrete oxide-passivated planar diodes and transistors provide a high level of component reliability. By combining a number of components into integrated circuits in and on single silicon wafers and enclosing entire circuits in packages of the size previously used for single components, the circuit reliability is further improved. At present, the reliability of an entire integrated circuit is about the same as that of a single discrete component in a nonintegrated circuit.

The active devices in most microcircuits have been bipolar transistors and diodes. Semiconductor technology and the understanding of semiconductor surface properties have been developed to a point where a recently-developed class of insulated gate field effect transistors, known as MOS transistors, provides an alternative to bipolar devices. These field effect transistors offer advantages over bipolar transistors for certain applications. These advantages include low standby power levels, high input impedance, low noise level at high frequencies, relative insensitivity to temperature, absence of thermal runaway, and simplicity of circuit design. They do not require the isolation layers that are necessary with bipolar transistors, and they can be made in complex digital arrays with greater fabrication simplicity than can bipolar transistors.

1.2 Program Objectives

The objectives of this program were to develop the knowledge and understanding necessary for fabricating improved MOS transistors. The desired improvements included:

1. More stable electrical characteristics,

2. Lower threshold voltage,

3. Improved resistance to ionizing radiation.

The information generated in this program can also be applied to the broader area of silicon microcircuitry, since both MOS and bipolar devices and circuits are sensitive to the physical and chemical behavior of the silicon surface covered with an oxide and an overlying metal.

The performance of both MOS and bipolar devices at very low power levels is very dependent on the properties of the silicon surface. The improvements in understanding of the silicon surface properties, made possible by MOS analytical techniques, provide a basis for making improved devices for low power applications.

In an even broader field, the development of an improved understanding of oxides provides a basis for the study and development of other possible insulating materials in MIS (metal-insulator-silicon) devices.

One of the problems in understanding the behavior of MOS devices has been the fact that various investigators have attempted to explain their observations in terms of a single simple model. Such attempts to simplify some very complex mechanisms are laudable and do contribute to the over-all understanding. However, of the many references listed in Appendix A, there is none that combines, organizes, and analyzes the many sources of information which are relevant to the objectives of this program. On the one hand, investigators who have been very successful in explaining the instability due to alkali ions have never mentioned the effects of hydrogen and/or water. On the other hand, others have discussed the effects of hydrogen and water without mention of the effects of alkali ions. One objective of this program was to organize, analyze, and inter-relate the scattered observations and interpretations in the rapidly growing literature to provide a fairly unified picture of MOS phenomena.

1.3 Description of Basic MOS Structure

MOS devices make use of the fact that the surface potential and therefore the density of charge at a silicon surface covered by an oxide can be controlled by the voltage applied to a metal electrode on the oxide. The net charge in the silicon consists of immobile ions in a depletion layer and mobile carriers either in an accumulation or an inversion layer. More specifically, with n-type silicon, a positive voltage on the metal attracts electrons to the surface of the silicon, forming an accumulation layer of electrons. A negative voltage on the metal repels electrons and forms a depletion layer in n-type silicon. As the voltage applied to the metal is made more negative, mobile positive carriers (holes) form an inversion layer at the silicon surface within the depletion layer. This is illustrated in Figure 1.

The depletion and inversion layers play important parts in determining the electrical behavior of MOS capacitors and transistors.

1.4 MOS Transistors

In an MOS transistor, the inversion layer forms a channel (conductive layer) in which the conductance can be controlled. This channel is located between a source region and a drain region as shown in Figure 2, and its conductance can be varied by varying the voltage applied to the gate electrode. It is characteristic of the currently fabricated MOS transistors that the surface potential of the silicon is negative in the unbiased condition. That is, a layer of electrons is present along the silicon surface. This is the reason that an undesirably high (threshold) voltage must be applied to the gate to make a p-channel MOS transistor conduct or to make an n-channel transistor nonconducting. Transistor threshold voltages can also be high because of traps at the silicon surface which immobilize carriers in the inversion layer.

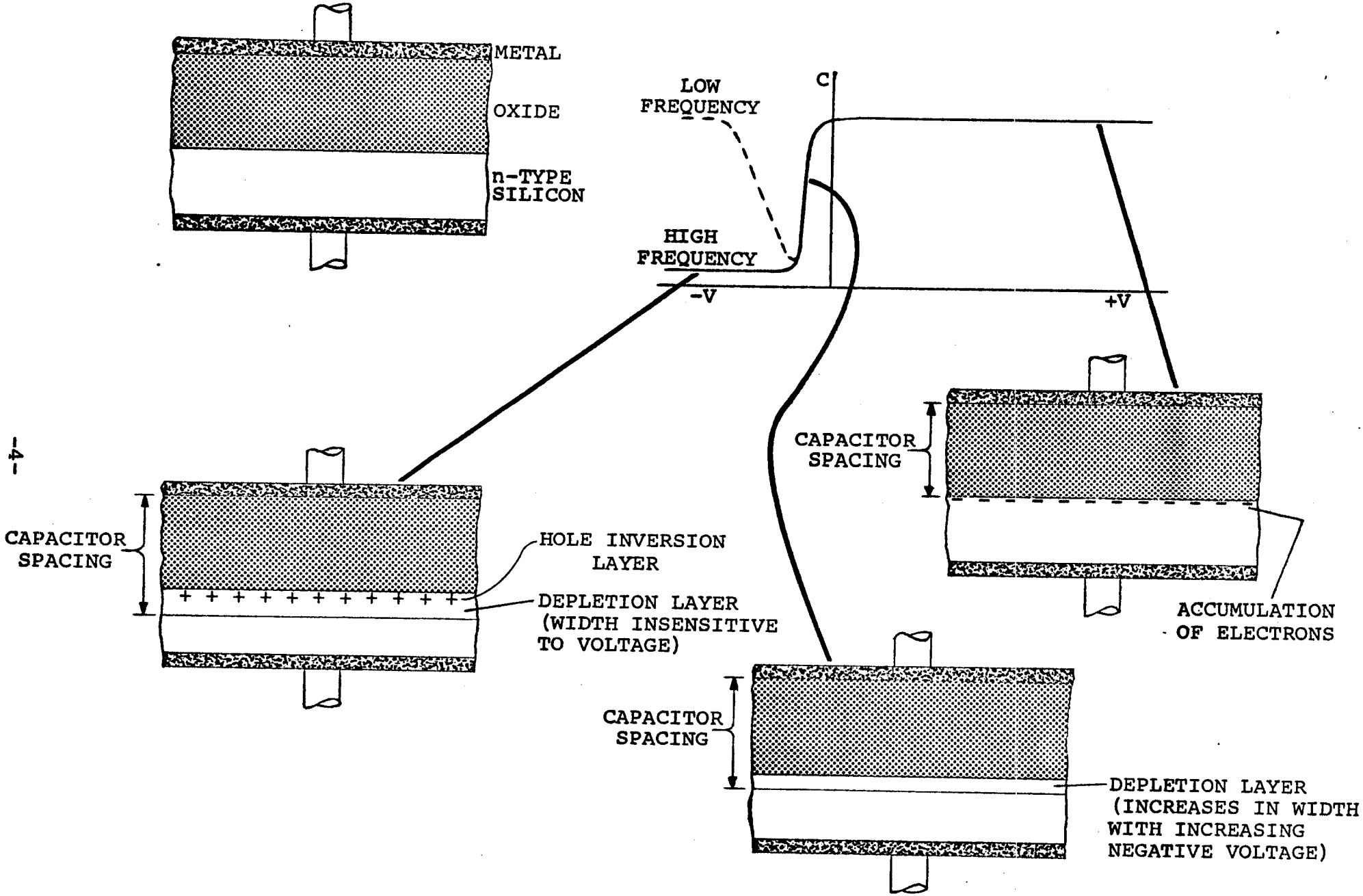


Figure 1. Capacitance-voltage relationship of MOS capacitor.

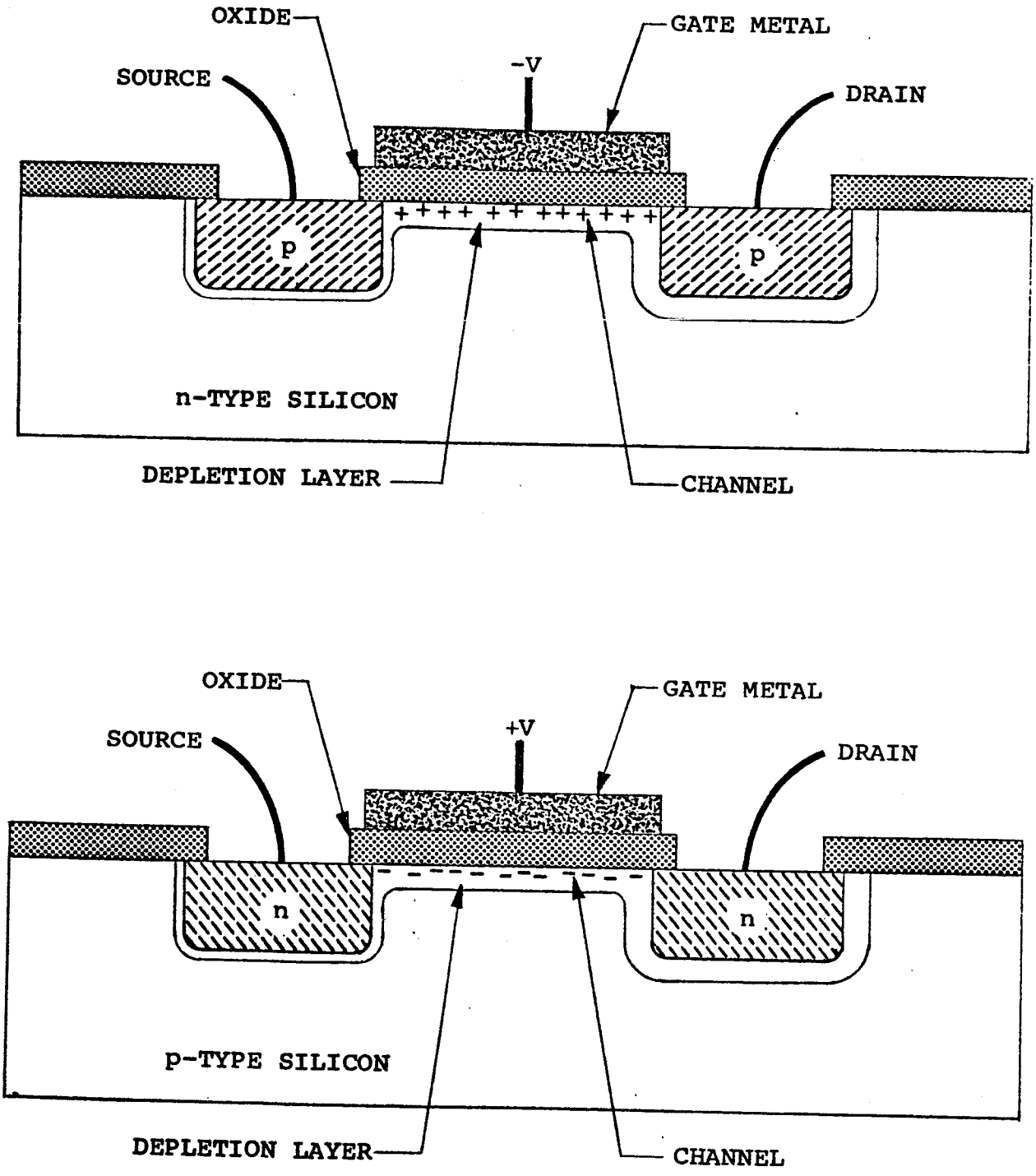


Figure 2. MOS transistor structure.

1.5 Basic Physics

Consideration of the basic physics involved in an MOS structure leads to the following understanding of the influence of charge in the oxide on the properties of an MOS device. For a given silicon impurity density, the capacitance of a depletion layer of an MOS capacitor or the conductance of an inversion layer of an MOS transistor is uniquely determined by the surface potential of the silicon. In the interior of the silicon (beyond any depletion layer or accumulation layer), and in the metal, the conductivities are sufficiently high that the electric field may be assumed to be zero. The net area density of charge in the region between the interior of the metal and that of the silicon is zero according to Gauss' law. Since the relationships between voltage, fields, and charge densities are linear, the effect of charge in the oxide on the charge density in the silicon can be considered independently of any applied voltage or contact potentials. That is, we can consider the influence of oxide charge on the surface potential of the silicon, which determines the charge density in the silicon, and then separately take into account the applied voltage and the contact potential which add linearly to the surface potential and to the charge density.

To illustrate, assume a layer of charge of uniform density located on a plane in the oxide as shown in Figure 3. Note that the total charge density, i.e., the sum of the charge densities in the metal, the oxide and the silicon is equal to zero. From these charge densities one can calculate the distribution of the electric field using Gauss' law. This is illustrated in Figure 4. The area under the field curve is equal to the applied voltage plus the contact potential. To simplify the discussion we assume that the voltage across the oxide, i.e., the applied voltage plus the contact potential is zero.

If the charge density in the oxide is increased at the same location, the charge density in the silicon (and that in the metal) increases because of the requirement that the net charge density per unit area must be zero.

If the oxide charge density remains constant and the charge is moved toward the silicon, the density of the charge in the silicon must increase and that in the metal must decrease so that the field between the oxide charge and the silicon increases and that between the metal and the oxide charge decreases as required to maintain the over-all potential drop across the oxide at zero.

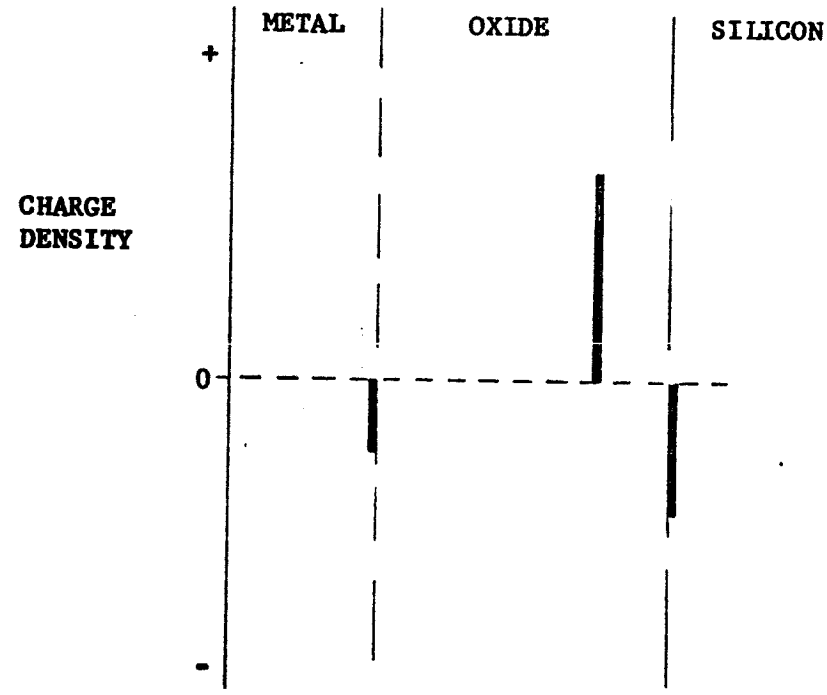


Figure 3. Assumed charge distribution.

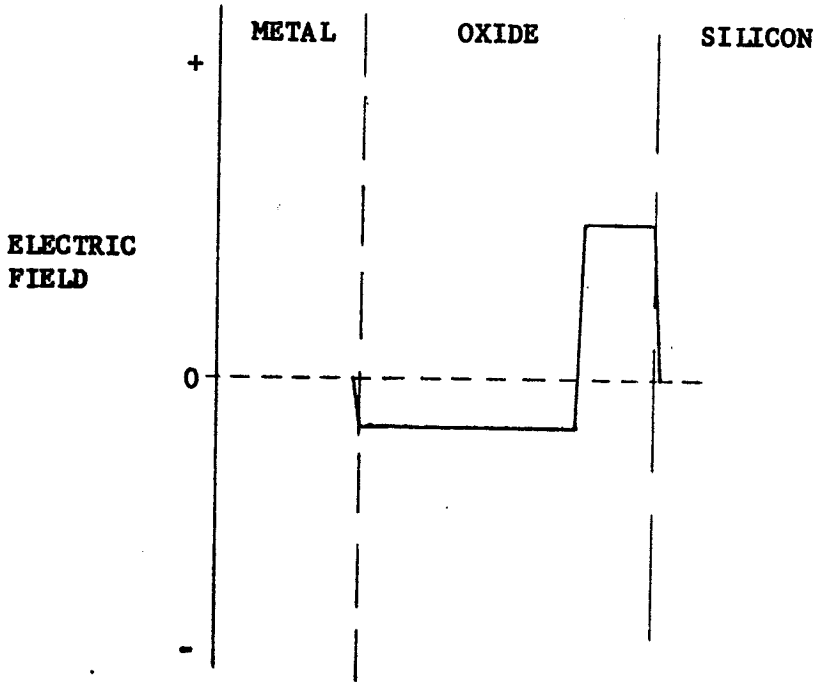


Figure 4. Electric field distribution.

Because the relationships involved with the charges, the fields, and the voltages are linear, the above considerations can be extended to distributions of charge throughout the oxide.

The points discussed above may be summarized as follows:

1. An increasing density of oxide charge induces an increasing area density of charge in the silicon.

2. A movement toward the silicon of a fixed amount of charge in the oxide increases the density of the charge in the silicon.

The effect of an applied voltage and of the contact potential is to apply an additional voltage drop across the oxide, thus adding a given number of charges per unit area to the metal and an equal number of charges of the opposite sign to the silicon. The polarity of these charges is determined by the polarity of the voltage across the oxide.

The capacitance of the depletion layer, or the conductance of the inversion layer, in an MOS device is determined by the surface potential of the silicon. This surface potential, for a given volume density of impurity atoms in the silicon, is uniquely related to the area density of charge in the silicon. The area density of charge in the silicon depends independently and, therefore, interchangeably on the applied voltage, the contact potential, and the distribution of charge in the oxide. The contact potential is constant and fairly well determined (Grove et al[67] show it to be zero for n-type silicon and 0.7 V for p-type silicon, each having 10^{16} atoms/cc). Whelan[242] has published in useful graphical form the relationship between the capacitance in the silicon and the silicon surface potential. A comparison of the theoretical curve and an actual measured curve can be used to calculate an <u>effective</u> density of charge in the oxide, based on the knowledge that the effects of charge and applied voltage are interchangeable and an arbitrary assumption that the oxide charge is entirely located at the oxide-silicon interface.

1.6 General Model

Figure 5 is an attempt to show in one drawing all of the types of charge of importance in this program.

The density of immobile charge in an oxide establishes a lower limit on the threshold voltage of a transistor. In this report we consider the immobile charge to be the charge remaining after a negative voltage has been applied to the metal at an elevated temperature to drift any mobile charges away from the silicon.

Mobile ions in the oxide or on the oxide cause device instability.

A trap can be defined as an allowed state that exists in the energy gap that can capture either a hole from the valence band or an electron from the conduction band and hold it for a period of time before it returns it to the energy band from which it came. This can be contrasted with a recombination center, which is a level that can capture an electron from the conduction band and after a period of time give it up to the valence band. Traps are usually characterized as fast or slow according to the time constant involved with their filling and emptying. This time constant is dependent on the energy difference between the level of the trap in the energy gap and that of the edge of the gap, and it is dependent on the density of mobile charges in the band from which the charges are captured. This density of charges depends on the potential energy at the trap site, the temperature, the presence of ionizing radiation and the spatial distance from a region in which there is a more abundant supply of the carriers. On this last point, for example, carriers from the conduction band of the silicon can tunnel into traps in the energy gap of the oxide if they are located sufficiently near to the silicon.

Traps have several important effects in MOS devices. The filling and emptying of slow traps changes the charge distribution in the oxide and causes the device properties to change, making the device unstable. If the time constant is shorter, the occupancy of the traps may change in the time during which a characteristic curve is measured, altering the curve shape. Fast

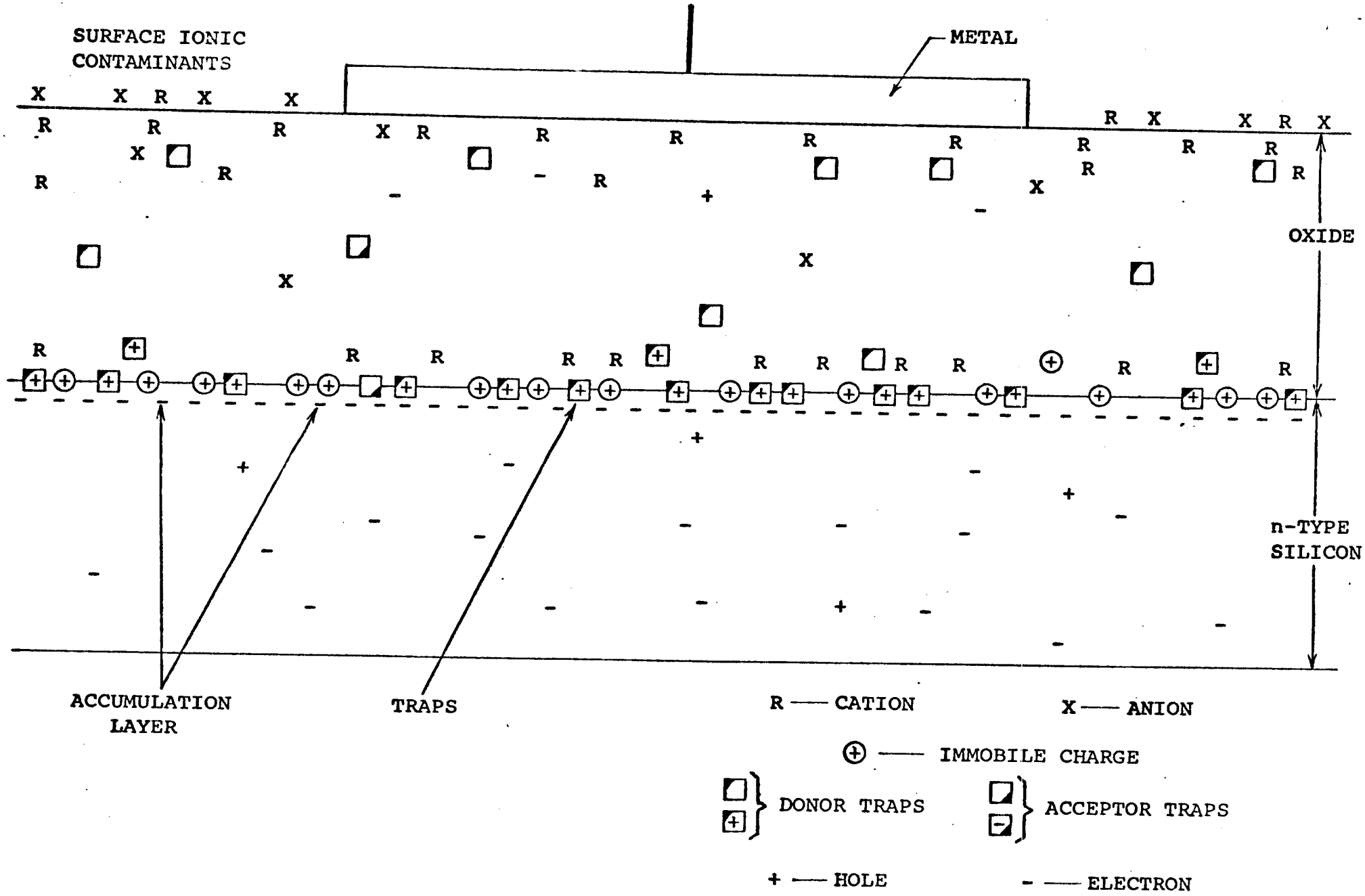


Figure 5. Distribution of charges in a MOS structure.

traps can capture carriers for short periods of time and immobilize them so that they cannot contribute to a current when an electric field is applied. These traps reduce the transconductance of a transistor and can reduce the Q of a capacitor.

The most sensitive effect of ionizing radiation is the charging of traps in the oxide; and therefore traps play an important part in determining the radiation resistance of a device.

1.7 Scope of Report

The body of this report presents the important finings in this program with our interpretations and the related information from the works of other investigators. The references given in this report are listed at the end of the literature review included as Appendix A. The equipment and techniques used in this program are described in the next section. The remainder of the body of this report has been divided into four main parts: 1) instability, 2) threshold voltage, 3) radiation resistance and 4) the effects of water.

Appendix B contains most of the data on which the body of this report is based. The remaining data appears in the body of the report. Appendix C contains device structural data, and Appendix D contains a report prepared by a specialist in the field of glass technology.

2. EQUIPMENT AND TECHNIQUES

In addition to the regular equipment and techniques in use throughout the microelectronics industry for cleaning, etching, oxidation, diffusion, photolithography and packaging, this program involved some special pieces of equipment and techniques described in this Section.

2.1 Oxide Preparation

It has been shown by a number of investigators[88,112,114,276] that small amounts of water in the oxide significantly influence the properties of MOS devices, particularly those related to surface states. Most of the silicon oxides evaluated in this program were prepared by thermal oxidation in dry oxygen in an open-ended radiant heated quartz oxidation tube. In this system an oxide can absorb a significant amount of water when it is cooled at the gas outlet end of the oxidation tube where some room air can backflow into the tube. To thermally grow oxides containing a minimum amount of water an oxidation tube was modified so that a ground glass fitting can be opened at the end of the tube at which the dry gas (O_2 or N_2) enters the oxidation chamber. We are indebted to Dr. S. Hofstein of RCA Laboratories of Princeton, N.J. for suggesting this simple but effective modification. This set-up permits one to push a sample that was thermally oxidized in dry oxygen to the gas-inlet end of the tube to be cooled to nearly room temperature before it is exposed to the moisture-containing room air. Figure 6 shows this modification on the inlet end of the tube.

Some of the oxides were prepared by vapor plating in the apparatus shown in Figure 7. Figure 8 is a schematic diagram of this apparatus. Two types of vapor plated oxides were prepared in this program - CO_2 oxides and SiH_4 oxides.

CO_2 oxides were prepared by the reaction[218]

$$SiCl_4 + 2H_2 + 2\,CO_2 \rightleftharpoons SiO_2 + 2CO + 4HCl$$

In this process, silicon wafers are placed on a carbon boat and the system is flushed with a large volume of hydrogen to purge any air from the reactor tube. The wafers are induction heated to 1050° C in a hydrogen ambient and then allowed to stabilize at that temperature for several minutes. The CO_2 gas and the $SiCl_4$ vapor are then introduced into the reactor. The halide vapor is

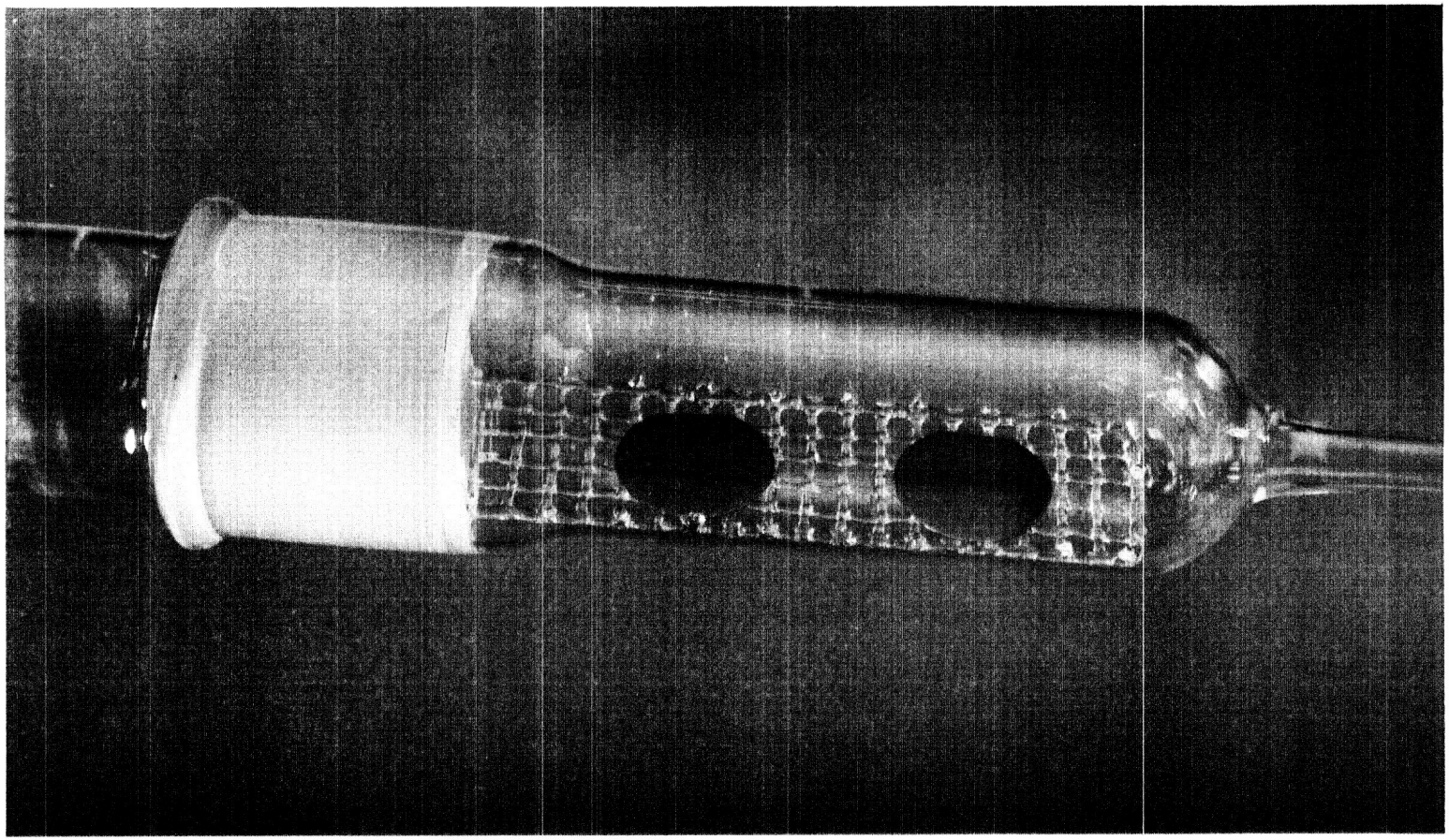


Figure 6. Modified inlet end of oxidation tube.

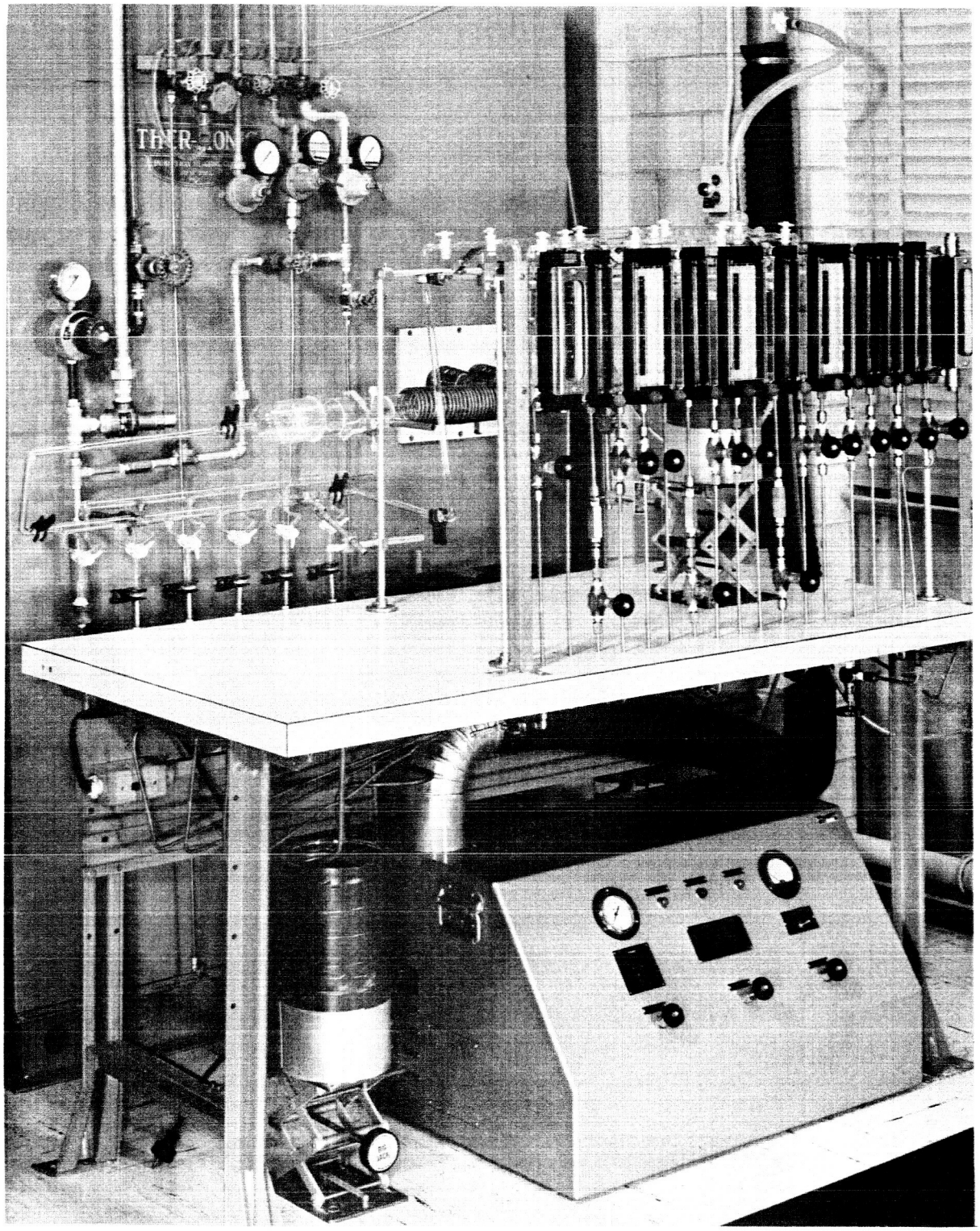


Figure 7. Vapor plating apparatus.

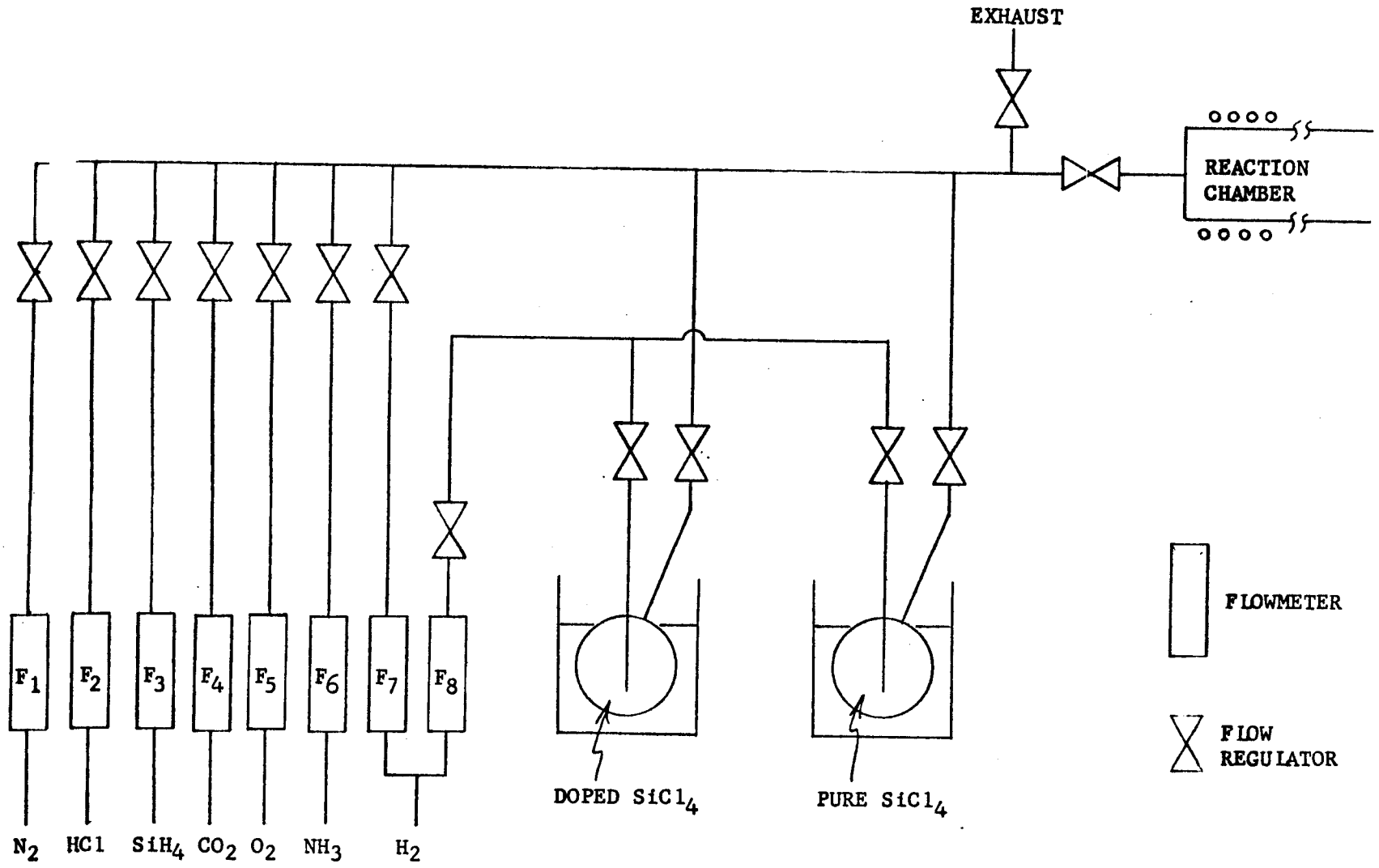


Figure 8. Schematic flow diagram of gas input system used for vapor plating experiments.

carried to the reaction chamber by passing a portion of the total hydrogen flow through a flask containing $SiCl_4$ held at 0° C to give the desired concentration (% volume) of $SiCl_4$ in the gas phase.

Typically the vapor deposition conditions were:

H_2 (mainstream)	10 l/min.
$SiCl_4$ @ 0° C	0.5 l/min.
CO_2	0.85 l/min.
Temperature	1050-1175° C

SiH_4 oxides were vapor deposited by the reaction[33]

$$SiH_4 + 2O_2 \rightleftharpoons SiO_2 + 2H_2O.$$

In this process silane is pyrolytically decomposed at high temperatures. In the presence of an oxygen-containing ambient an SiO_2 film is deposited on the hot silicon substrate. The silane is diluted with nitrogen to a concentration of less than 5% by volume to render it non-pyrophoric.

Typically the vapor deposition conditions were:

SiH_4	5 cc/min.
O_2	2.5 l/min.
N_2	26.8 l/min.
Temperature	830-1270° C

2.2 Silicon Nitride Preparation

Some of the data given in this report was taken on MNS capacitors made with silicon nitride layers that were prepared for another program with the apparatus shown in Figures 7 and 8. The reaction used for the vapor deposition of silicon nitride was

$$3SiH_4 + 4NH_3 \longrightarrow Si_3N_4 + 12H_2.$$

This reaction occurs at 900° C. The reaction occurs only on the hot silicon.

High flow rates of hydrogen were maintained through the tube during deposition to dilute the silane to a concentration of less than 5% by volume as a safety precaution.

Typically the vapor deposition conditions were:

SiH_4	6 cc/min.
NH_3	1.3 l/min.
H_2	100 l/min.
Temperature	830-940° C

The characteristics of some MIS capacitors made with these nitrides are reported in Section 5 and Appendix B.

2.3 C-V Measuring Equipment

The equipment for measuring the C-V relationship is shown in Figure 9. A schematic diagram is shown in Figure 10. The basic instrument for measuring the capacitance is a Tektronix L-C Meter that provides a direct reading measurement of the capacitance in the range of 0 to 300 pF at a measurement frequency of 140 kHz. The 10^6 ohm resistor isolates the power supply from the L-C Meter so that the capacitance of the power supply is not measured. The 0.01-μF capacitor prevents d-c current from flowing through the L-C Meter. The X axis of the X-Y recorder records the voltage applied to the device and the Y axis records the voltage at the terminals of the indicating meter in the L-C Meter. The current meter indicates any d-c leakage current through the capacitor.

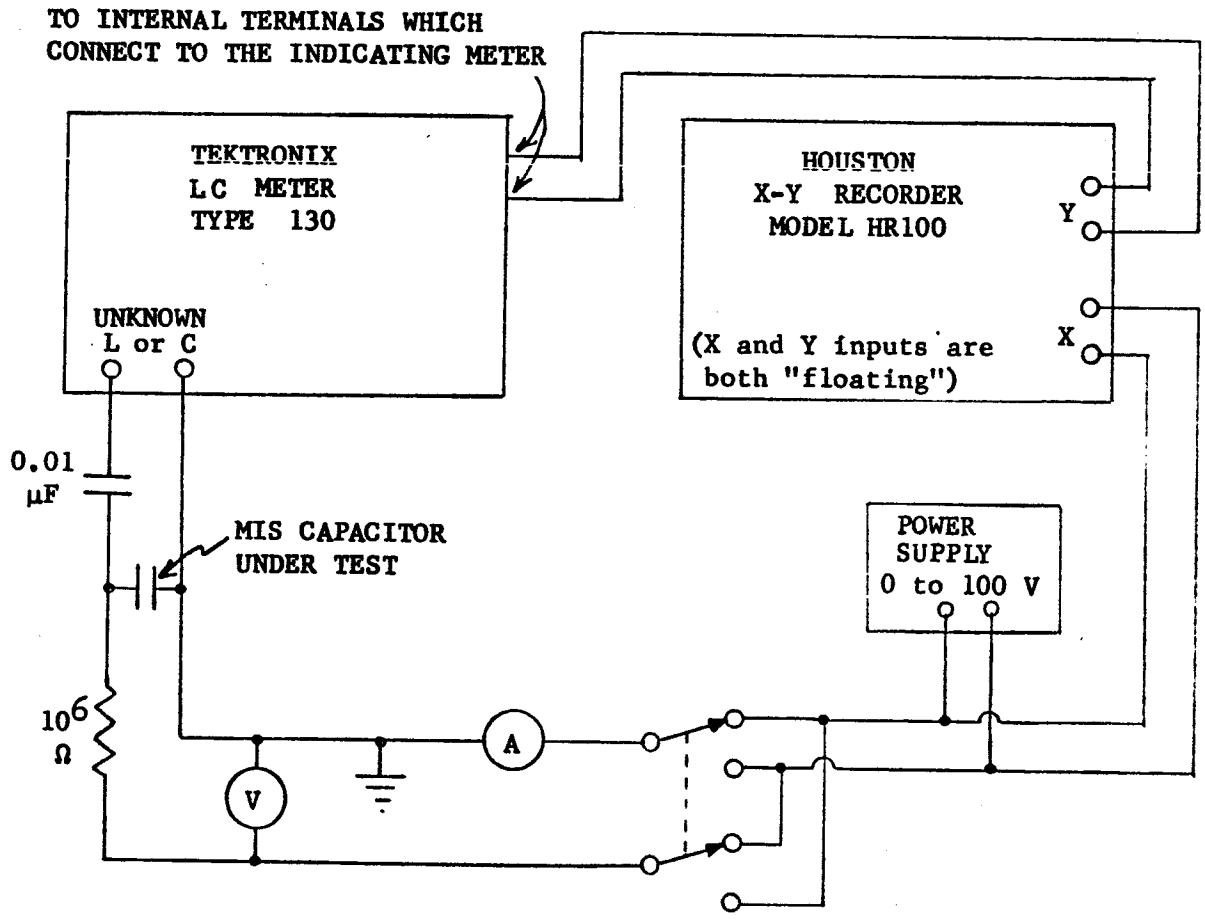
2.4 Equipment for Storage and Testing of Unpackaged Devices

To store and test the oxidized silicon wafers in a clean dry ambient, a gloved drybox was set up in which the samples were stored after oxidation and in which the unmetalized oxide layers were evaluated by means of C-V measurements. Figure 9 shows this drybox with the C-V testing equipment. Clean, dry nitrogen is constantly pumped into this drybox. There is an air lock on the right end of the drybox. Whenever the outer door is opened, there is an automatic sequence during which the air lock is evacuated of the room air and filled with dry nitrogen before the inner door can be opened. Figure 11 is a close-up photograph of the drybox and some of the testing equipment.

An effort was made to develop a technique for testing the C-V characteristics of nonmetalized oxides in wafer form. Indium and mercury contacts were evaluated with variable degrees of success. The best results were obtained with a method developed at Fairchild Semiconductor which makes use of a gold ball probe, as shown in Figure 12, which is firmly mounted on a micromanipulator and functions as a temporary, easily removable metal electrode to make a MOS capacitor of an unmetalized oxide. We found that good results could be obtained at room temperature with this gold ball probe.

We extended the use of the gold ball probe to drift testing at elevated temperatures. This capability permits the testing for the presence of mobile ions early in the processing sequence. This technique is most useful for the detection of serious contamination.

Figure 9. Equipment for measuring the capacitance-voltage relationship.



(A) Sensitive DC Meter,
Boonton Electronics Corp. Model 95A-R

(V) Electrometer, Keithley 610B

Figure 10. Diagram of equipment set-up for measuring C-V relationship of metal-insulator-silicon structures.

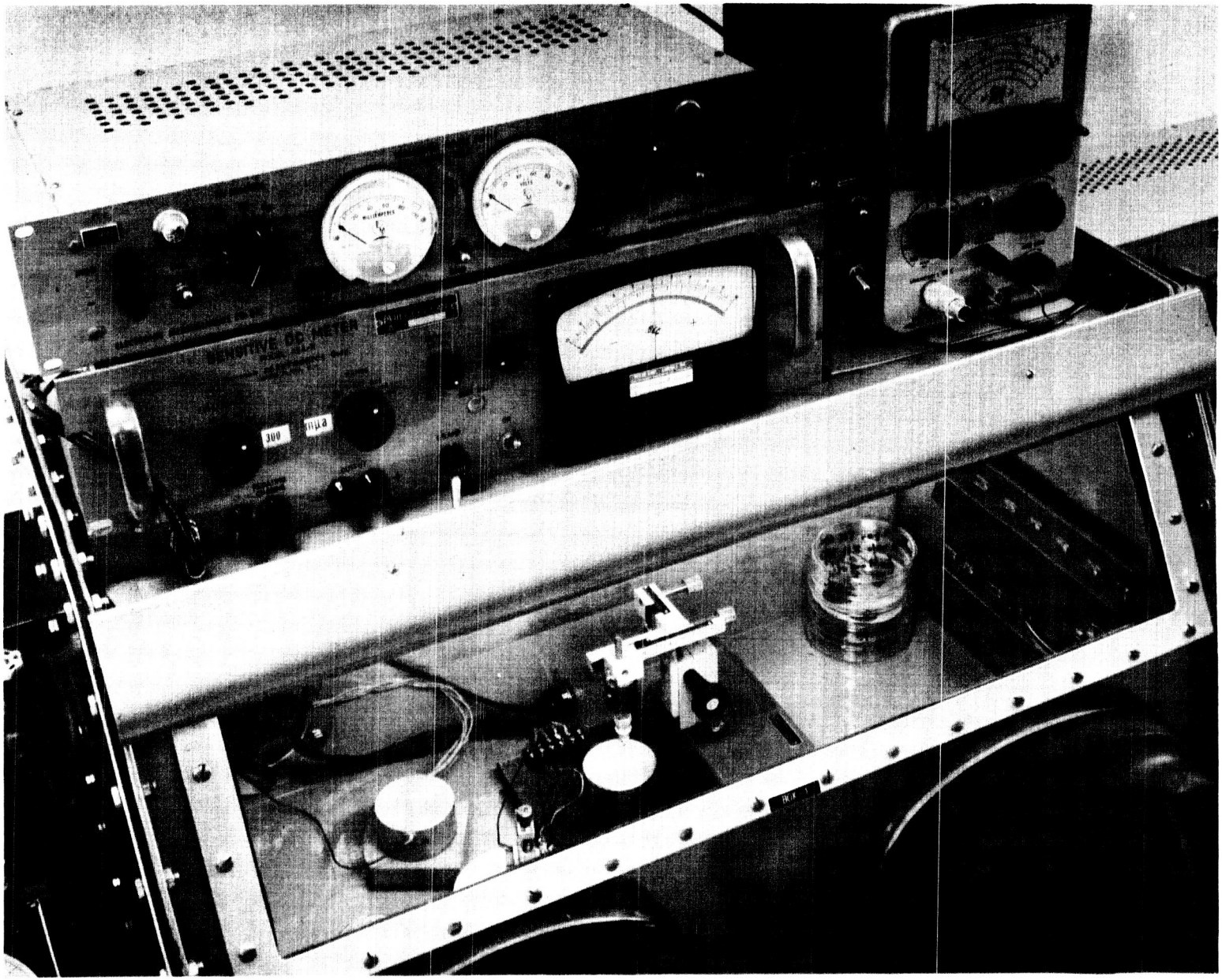


Figure 11. Close-up view of drybox and some of the testing equipment.

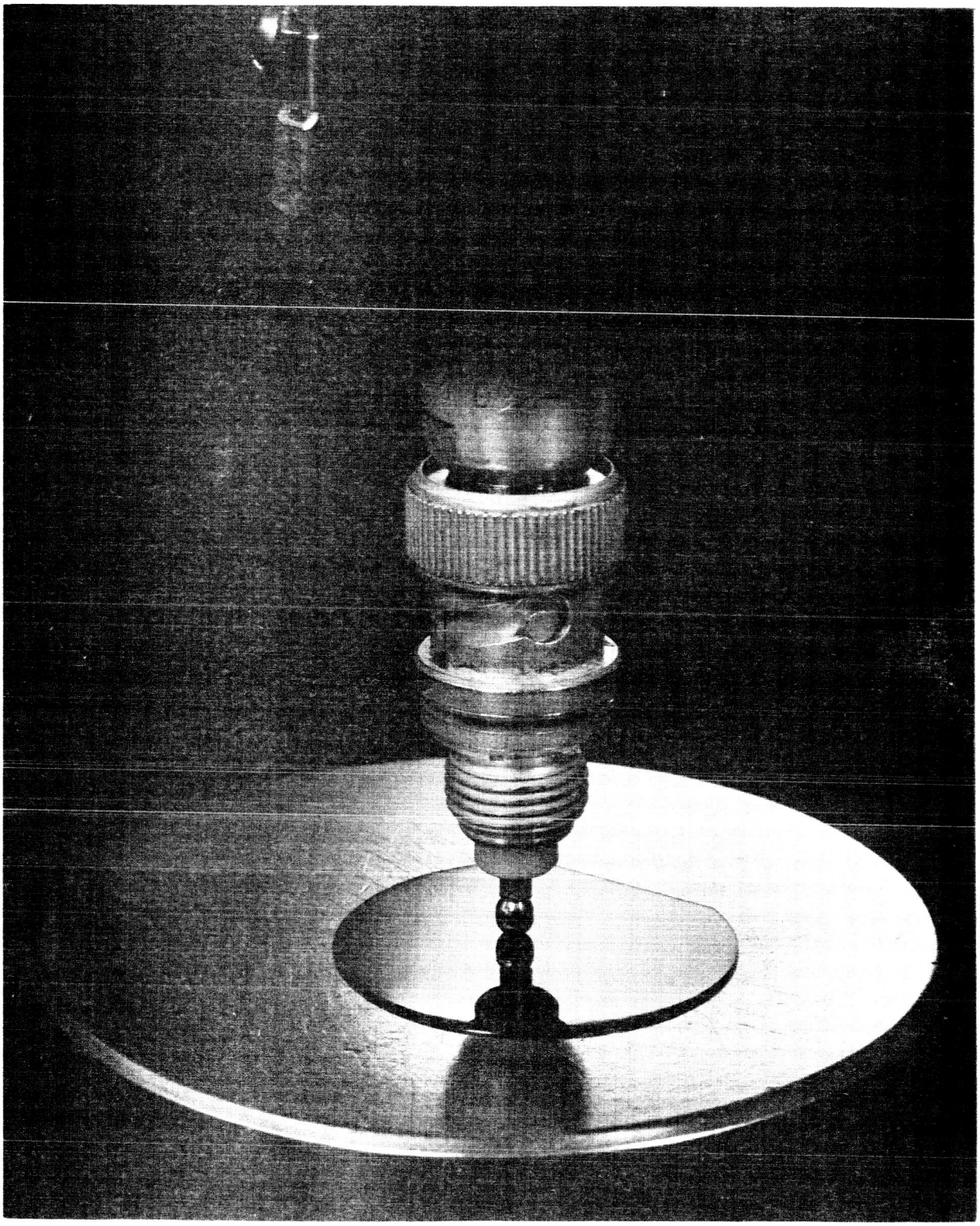


Figure 12. Gold ball probe for measuring capacitance-voltage characteristics of nonmetalized oxides in wafer form.

Precise measurements are made difficult by a number of problems. The necessary heating and cooling sequence causes a sufficient amount of relative movement at the probe contact so that the C-V curves are not always as well shaped or as reproducible as one would desire. Another frequent problem is one of leakage current through the oxide.

We also performed drift testing with large-area silicon wafers (Figure 13). This approach reduced the problems of sliding contacts and leakage current. In this case, however, there is more uncertainty of the field strength applied across the oxide because of air spaces between the electrodes and the oxide sample.

2.5 Equipment for Testing Radiation Resistance

The Co^{60} source used for irradiating devices was made available at the University of Pennsylvania. The dose rate of this source was 7×10^4 rads/hour at the end of this program.

Figure 14 is a photograph of the electrical equipment used for testing transistors during the irradiation. This equipment uses a modified Tektronix type 575 Transistor Curve Tracer for measuring the transistor characteristics. A switching apparatus connects the transistors in parallel to the aging-bias power supply and removes this aging bias from one transistor at a time and connects the transistor to the curve tracer.

An alternative technique for measuring the transistors was to measure the drain current as a function of the gate-to-source voltage at a fixed frain-to-source voltage. The substrate was connected to the source.

The electrical measurements taken on capacitors during the irradiation were taken with the apparatus shown in Figure 15. It is the basic C-V curve measuring equipment shown in Figures 9 and 10 with the addition of a power supply for the aging bias.

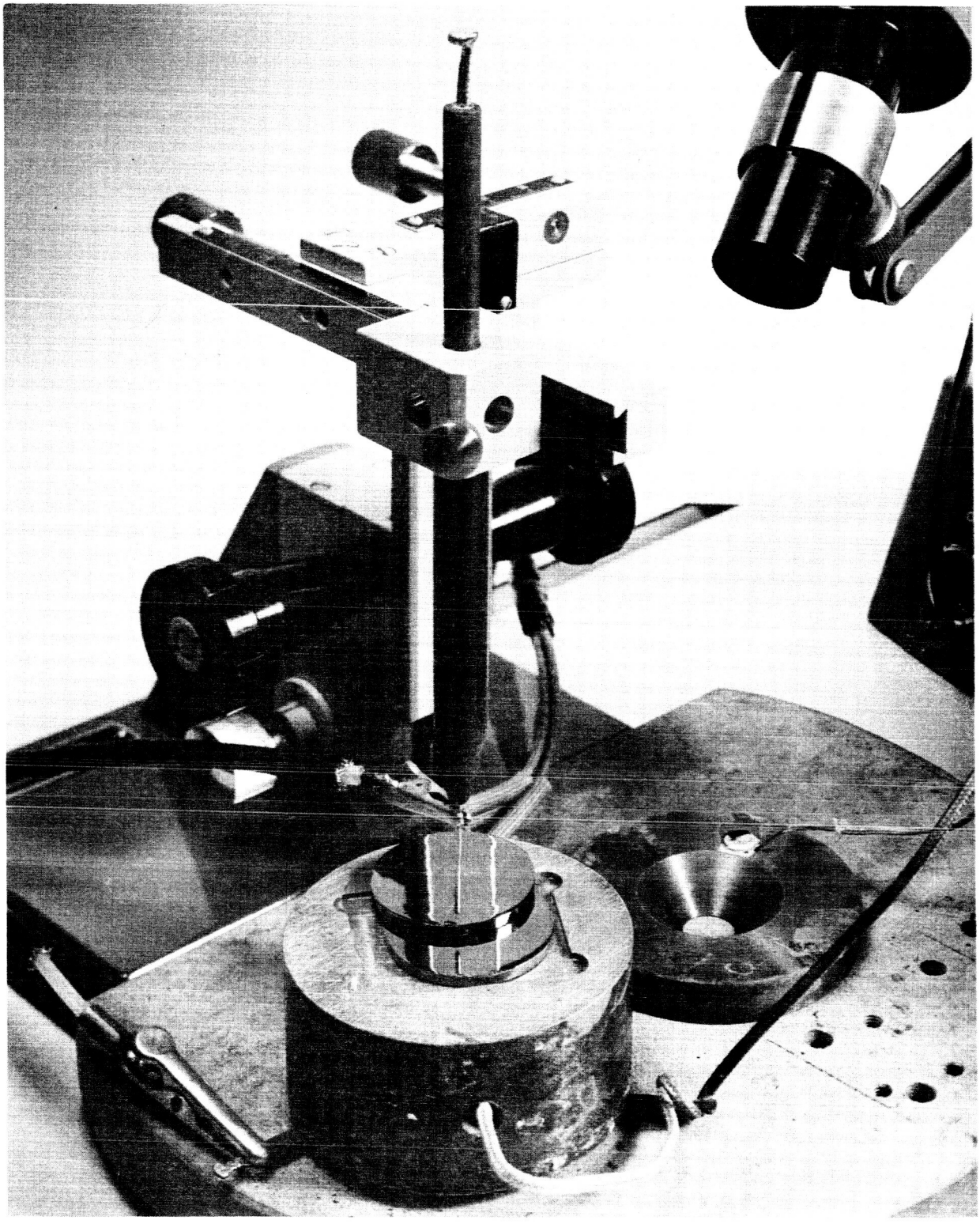


Figure 13. Large area silicon wafers for drift testing.

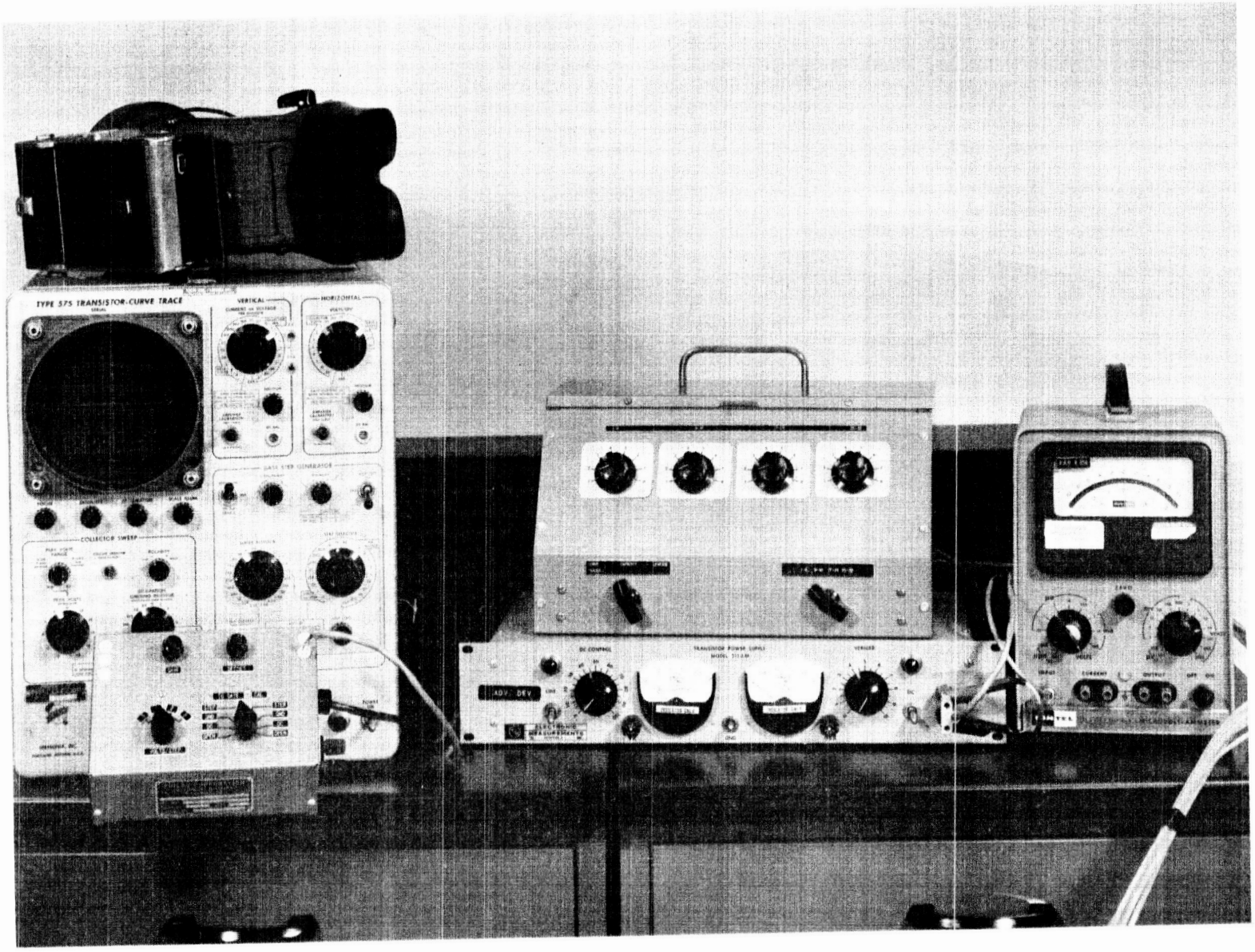


Figure 14. Electrical equipment used for biasing and testing transistors during irradiation.

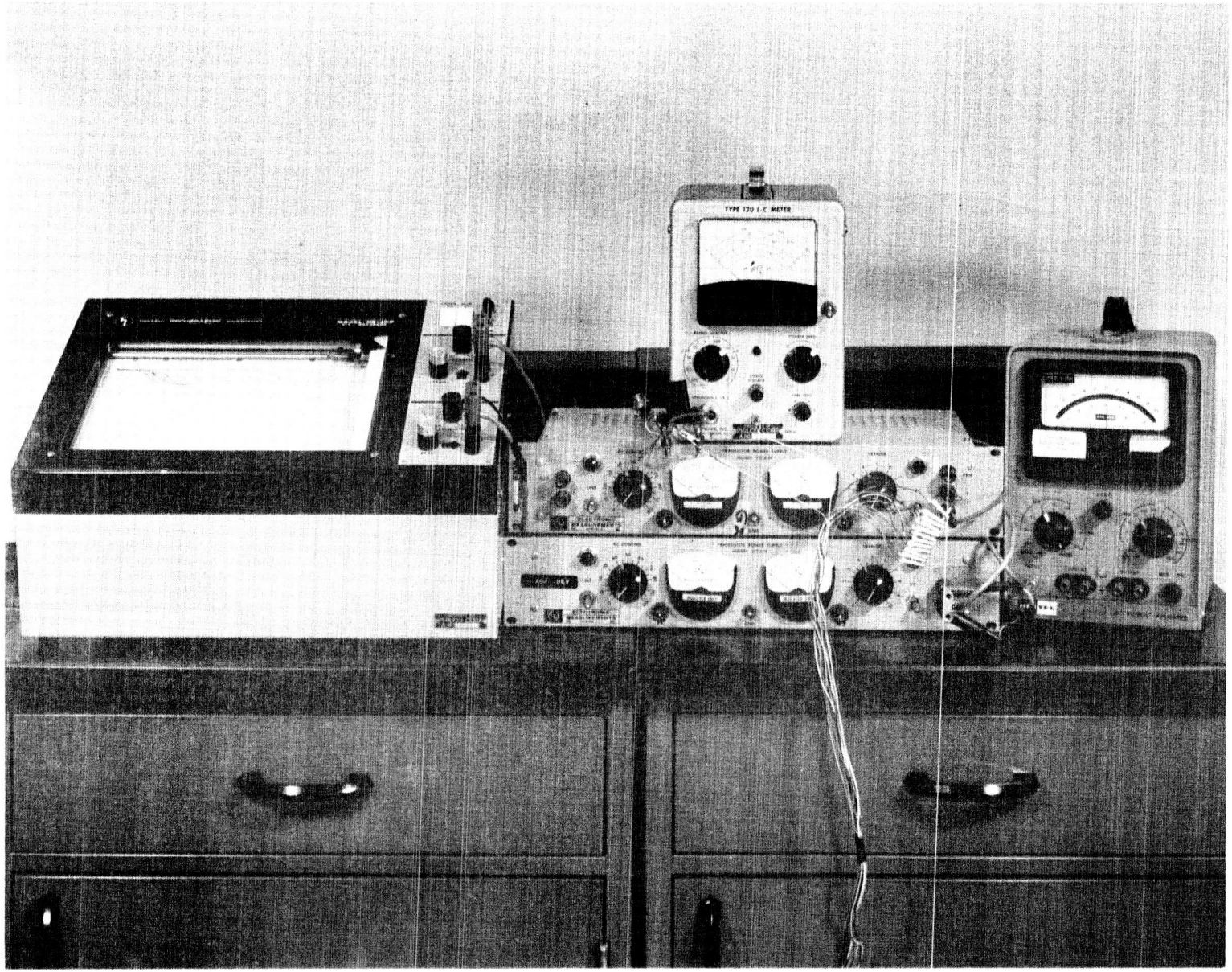
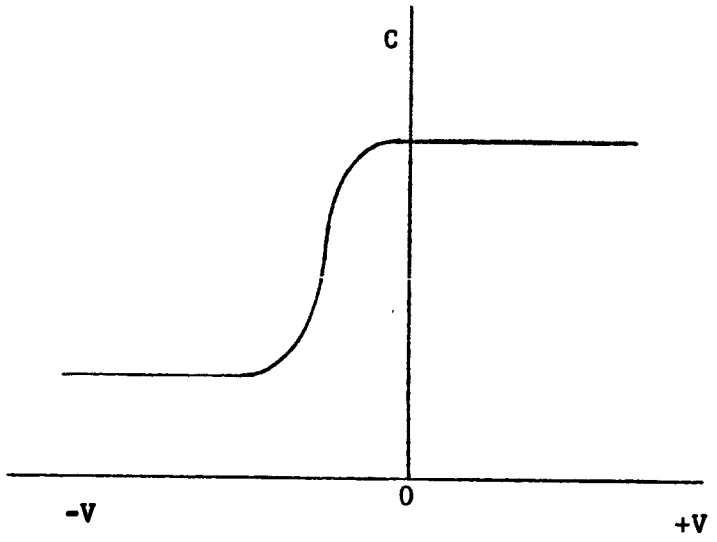


Figure 15. Electrical equipment used for biasing and testing capacitors during irradiation.

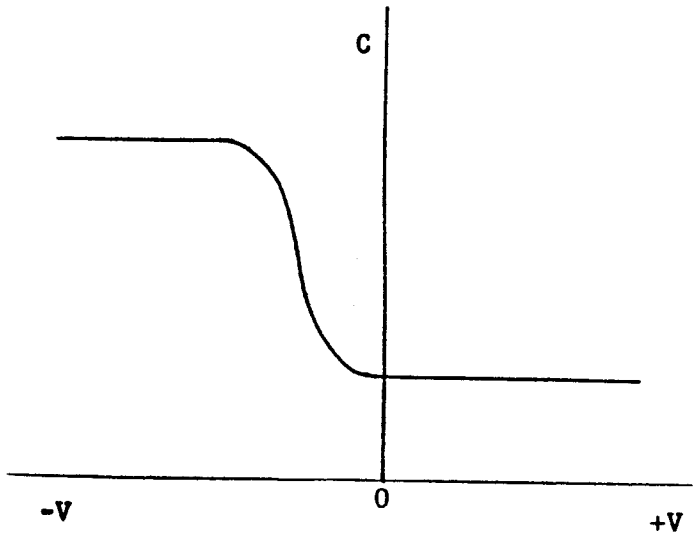
2.6 Charge Density Determination

The MOS capacitor is a useful tool for the study of the distribution and the behavior of charges in oxides on semiconductors. The characteristic capacitance-voltage relationship of an MOS capacitor at room temperature in the absence of intense ionizing radiation and at high measurement frequencies (i.e., higher than 1000 Hz for most oxides) has the general form shown in Figure 16. The transition region, for both p- and n-type silicon, is located in the negative voltage region.

The highest capacitance is attained when the applied voltage attracts the majority carriers of the silicon toward the oxide, forming an accumulation layer. In this case, the measured capacitance is that of a capacitor having the dielectric constant and spacing (thickness) of the oxide. As the voltage is changed and the majority carriers in the silicon are repelled from the oxide interface, a depletion layer forms in the silicon. The capacitance of the depletion layer in series with the capacitance of the oxide establishes a total capacitance that is lower than that of the oxide alone. This explains the decreasing part of the C-V curve. As the voltage is changed further, the depletion layer widens and the capacitance decreases until the surface potential of the silicon induces the formation of a layer of minority carriers at the silicon surface. This layer of minority carriers is known as an inversion layer. Further changes in voltage are supported by increases in the density of minority carriers in the inversion layer. For this reason, further changes in voltage are entirely impressed across the oxide. The voltage drop across the depletion layer remains unchanged and therefore the depletion layer thickness and the capacitance remain constant as the applied voltage is further changed. This situation exists when the density of carriers in the inversion layer is capable of change in a time period shorter than that of the sweep of the applied bias voltage during the measurement, and is not capable of change in a period of the capacitance measurement signal. If the sweep time of the applied bias voltage is sufficiently short (e.g. less than a second for a typical oxide), so that there is insufficient time for the inversion layer to form during the measurement, then the leveling off of the capacitance at the lower-capacitance portion of the curve is not observed. On the other hand, if the measurement frequency is sufficiently low that the inversion layer charge density can change during the period of the measuring signal, then



a. n-type silicon



b. p-type silicon

Figure 16. General form of capacitance-voltage relationship of MOS capacitor.

the variations of the voltage that make up the measuring signal are supported entirely by the variations in charge density in the inversion layer. In this case, changes in voltage are applied only across the oxide and therefore the depletion layer does not contribute to the measured capacitance. In this case, only the capacitance of the oxide is measured. These three situations are depicted in Figure 17, for n-type silicon.

Since the time required to form carriers for the inversion layer depends on the temperature and on the presence of any ionizing radiation, the sweep rate and signal frequency at which different curve shapes are observed depends on the conditions of temperature and radiation. Figure 17 illustrates the limiting cases; actual curve shapes frequently lie between these extremes. Similar differences exist from sample to sample due to differing densities of carrier generation sites.

There are situations in which one observes the low frequency curve shape at relatively high measurement frequencies. This occurs when there is a large supply of carriers of the type that make up the inversion layer in the region laterally bounding the MOS area. Carriers from such a supply can move into and out of the MOS area at a more rapid rate than that at which carriers can be generated in the MOS area. The source of carriers in the region bounding the MOS area may be a p-n junction or an inversion layer, as illustrated in Figure 18.

Most commonly, low frequency curves are found at relatively high frequencies when the C-V curve is plotted for the gate-to-substrate capacitance of an MOS transistor or when the C-V curve is plotted for an MOS capacitor on p-type silicon (because of the surface inversion layer often found in p-type silicon).

The most useful conditions for evaluating the state of charge in the oxide are those that produce the middle curve in Figure 17. From C-V curves of this type, one can obtain the following information.

1. The oxide thickness can be calculated from the measured maximum capacitance per unit area using the equation

$$t_{ox} = \frac{\varepsilon_{ox}}{C_{ox}}$$

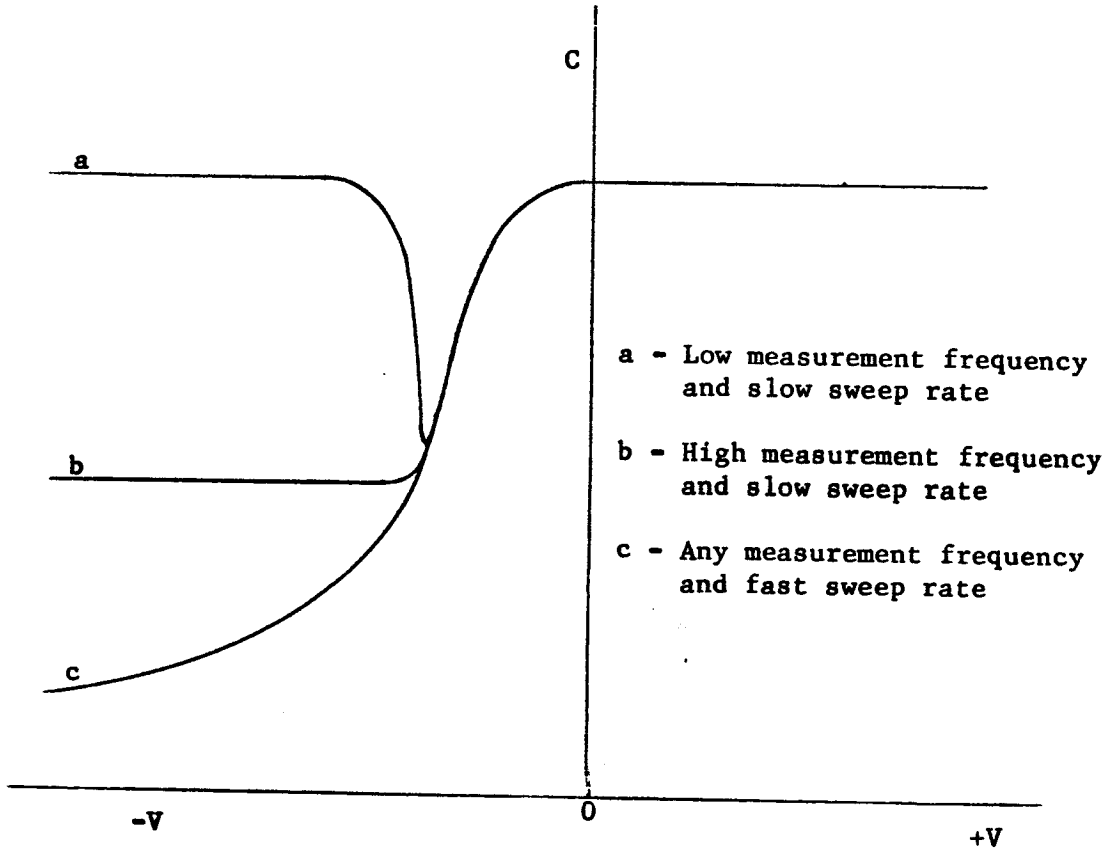
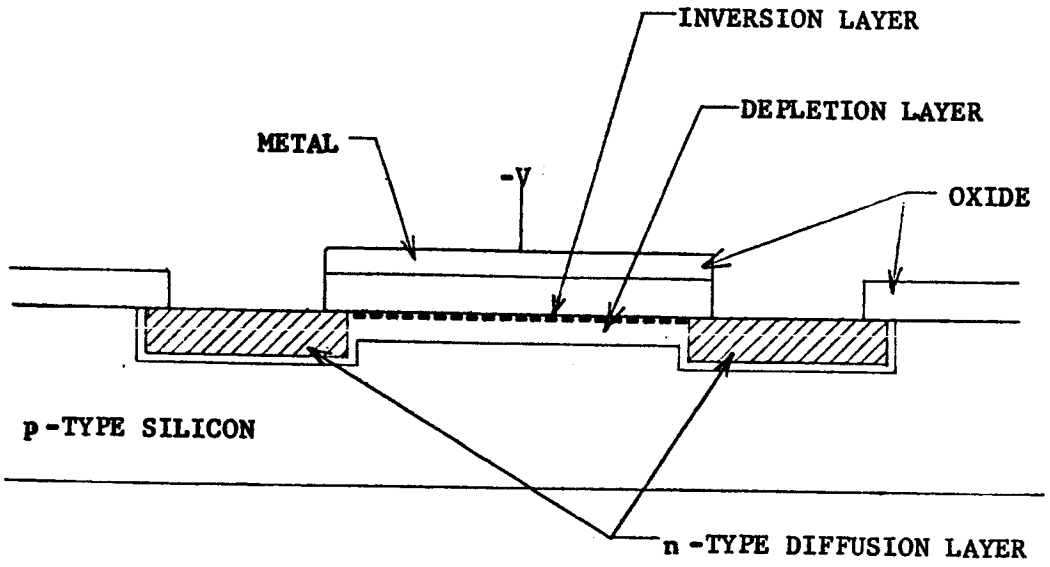
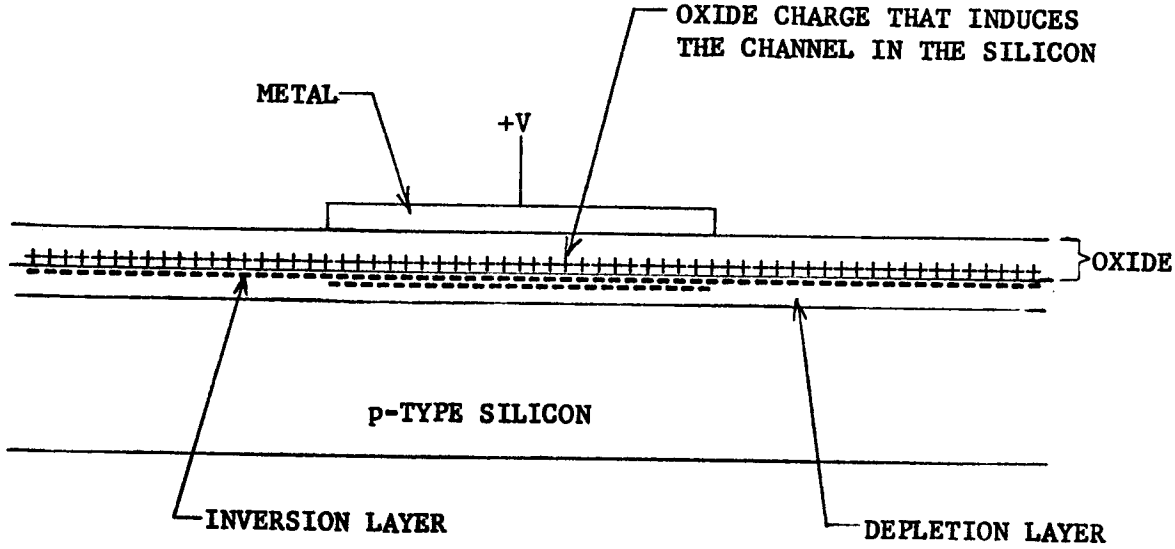


Figure 17. Variations in capacitance-voltage relationship due to differences in measurement signal frequency and sweep rate.



a.



b.

Figure 18. Illustrations of structures that exhibit low frequency capacitance-voltage curves at relatively high measurement frequencies.

where ϵ_{ox} is the permittivity of the oxide (3.55×10^{-13} F/cm), and

C_{ox} is the capacitance per unit area of the capacitor in the regions of the C-V curve where only the oxide capacitance is measured.

We have obtained very good agreement between the values obtained with this measurement and those from other thickness measuring techniques, such as those involving the combination of counting light interference fringes (which gives an estimate to within approximately 1000 Å) and an observation of the color (which is accurate to within 100 to 200 Å), or the Talysurf (which is capable of accuracy to within 50 to 100 Å).

2. The minimum capacitance of the depletion layer can be determined from the measured minimum total capacitance by using the equation for the total capacitance for two capacitors in series.

3. The impurity density of the silicon can be determined from the minimum capacitance of the depletion layer by using the curves published by Whelan[242]. (It is assumed that the impurity density is uniform.)

4. The capacitance of the depletion layer in the silicon for the condition referred to as the flat band condition can be obtained from the values of oxide thickness and the impurity density in the silicon using the curves by Whelan[242]. In the flat band condition the conduction and valence bands of the energy diagram for the silicon are flat out to the silicon surface. In this condition, there is zero space charge in the silicon. In the absence of oxide or interface states whose occupancy depends on the applied voltage, the density of charge on the metal at flat band condition is equal to the net charge density in the silicon at zero bias.

5. The flat band voltage can be obtained at the point on the C-V curve for which the capacitance is that of the flat band condition.

6. The effective charge density can be calculated from the equation

$$Q = C_{ox} V_{FB}$$

where C_{ox} is again the capacitance per unit area of the oxide, and V_{FB} is the flat band voltage. This calculation is based on the assumption that all of the effective charge is at or near the oxide-silicon interface.

With this basic approach, the effective charge density can be measured after each set of treatment conditions to separate the effects due to the different kinds of charge.

To separate the various kinds of charge, measurements of the effective charge density were made as outlined above after each of the following treatments:

1. A ten-minute warm-up period to 300° C followed by a -12 V bias on the metal for two minutes which was maintained on the device during cooling and up to just before testing.

2. Same as above with +12 V instead of -12 V.

3. A -12 V bias for five minutes at room temperature.

The immobile charge density is the effective charge density calculated after treatment 1. The change in the effective charge density due to treatment 3 we call the room-temperature-mobile ion density or RT ion density. The alkali ion density is the difference between the effective charge density after treatment 3 and that after treatment 1.

Mobile ions increase the effective charge density during treatment 2 and decrease it during treatment 3. If treatment 2 causes a decrease or treatment 3 an increase in charge density the instability is due to trapped charge.

A technique for separating the effects of mobile and trapped charge is described in subsection 3.8. In Section 6 we show how the slope of the C-V curve is a measure of the density of slow traps in the oxide.

3. INSTABILITY OF MOS DEVICES

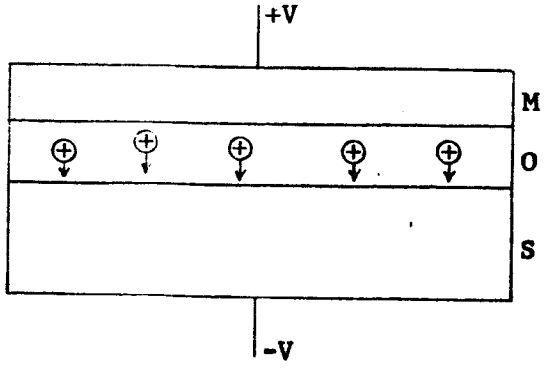
3.1 Model for Instability Due to Mobile Charge Within the MOS Structure

If a positive voltage is applied to the metal electrode of an MOS structure it causes any mobile charges in the oxide to drift in the direction that increases the positive charge density in the oxide in the region adjacent to the silicon. As described in subsection 1.5 the movement of positive charge through the oxide toward the silicon increases the negative surface potential of the silicon. The surface potential of the silicon determines the capacitance of the depletion layer in an MOS capacitor and the conductance of an inversion layer in an MOS transistor.

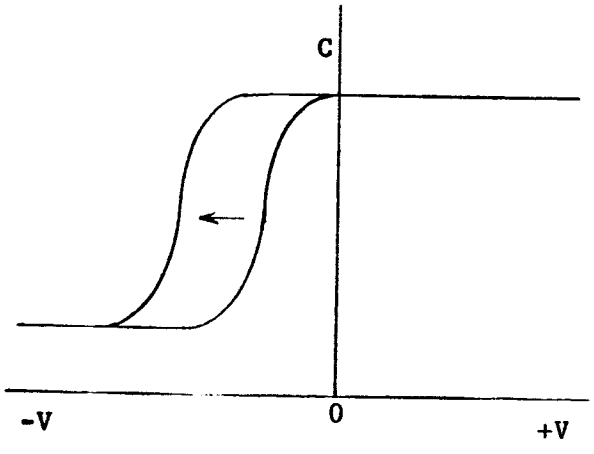
The movement of charge in an oxide causes capacitor or transistor characteristics to shift along the metal-to-silicon voltage axis as shown in Figure 19.

3.2 Alkali Ions

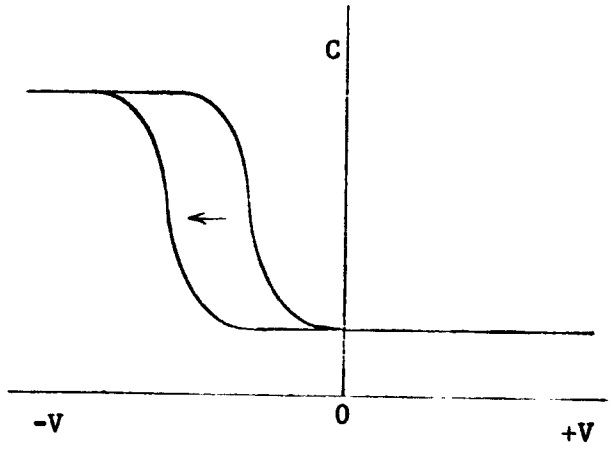
Snow et al[207] and Logan and Kerr[140] intentionally contaminated oxides with alkali ions to show that these contaminants can cause the type of instability that has been a major problem in the industry. Snow et al find that the charge induced in the silicon during a treatment, at a constant elevated temperature and constant positive applied voltage on the metal, is proportional to the square root of the drifting time until a saturation level is reached. This saturation level appears to be independent of the temperature. The activation energy for drifting the sodium ions in these samples is 16 kcal/mole (0.7 eV) and that for lithium contaminated samples is 11 kcal/mole (0.48 eV). They show that the 16 kcal/mole activation energy obtained for sodium from the square-root-of-time relationship is equivalent to an activation energy of 32 kcal/mole for the diffusion constant. This compares favorably with the value of 31 kcal/mole found by Owen and Douglas[170] for steady state conduction of sodium ions in fused silica.



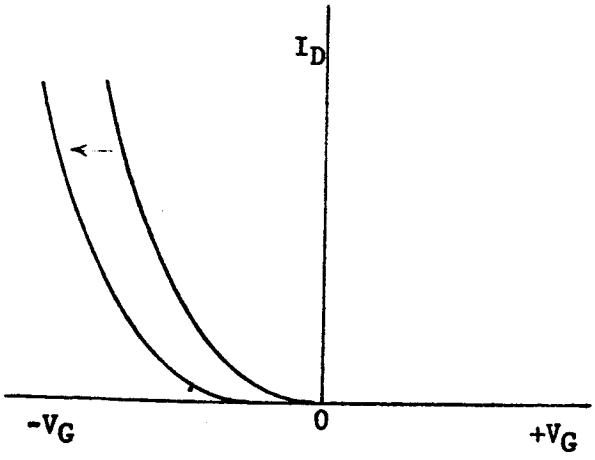
a. Ionic motion through oxide under applied field.



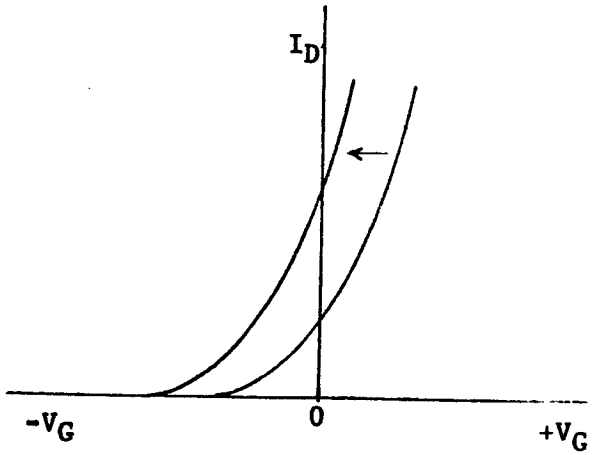
b. C-V characteristic of an MOS capacitor on n-type silicon.



c. C-V characteristic of an MOS capacitor on p-type silicon.



d. Drain current vs. gate voltage at fixed drain-source voltage for p-channel MOS transistor.



e. Drain current vs. gate voltage at fixed drain-source voltage for n-channel MOS transistor.

Figure 19. Effects of mobile charge on device characteristics.

Yon, Ko, and Kuper[250] have shown by means of radiochemical and MOS analyses that the distribution of sodium in the oxide can be quantitatively associated with the instability of MOS devices. In their experiments, the sodium concentration in the oxide within 1000 Å of the silicon interface correlates with the mobile charge found by MOS analysis in their samples. They found no instability without finding sodium. In ion drift experiments they found that changes in the relative distribution of sodium occurred mostly in the region within 1000 Å of the silicon.

Very recently, Williams[266] found, in studies of the photoemission of electrons from silicon into silicon dioxide following the sequential drifting of mobile ions through the oxide, that 2.1×10^{13} ions/cm^2 were located within 10 Å of the silicon.

One can infer from the studies by Yon, Ko and Kuper that when a large number of sodium atoms are introduced by diffusion the sodium atoms are not all ionized. It is not yet known why the ionized sodium atoms should be concentrated near the silicon. One might speculate that the stresses and discontinuities associated with the Si-SiO_2 interface influence the ionization energy of alkali ions.

Possibly the determining factor in establishing the distribution of ionized sodium atoms is the dependence of the probability for occupancy of an alkali atom on the electrostatic potential at its location. The presence of positive charge in the oxide sets up the condition in which the energy bands slope in the direction shown in Figure 20. This figure also shows that the deeper an atom is in the oxide in the direction away from the silicon the more likely a level due to an alkali atom is to be occupied. The levels due to alkali atoms are neutral when occupied and positively charged when empty. This may be a reason for finding most ionized atoms near the silicon. This hypothesis has not been evaluated in detail. No reference has been found for the ionization energy for sodium in silicon dioxide. Using the data given above by Williams, one can calculate by Poisson's equation that a uniform distribution of 2×10^{13} ions/cm^2 in a layer 10 Å thick establishes a voltage drop of 0.45 V across the 10 Å thick layer. One might expect the ionization energy to be within an order of magnitude of 0.45 V.

Phase III of the Scope of the Work in the contract called for the development of techniques to remove mobile ions from the oxide to create stable devices. It had been proposed that the contaminating ions might be drifted to the top surface of the oxide in an applied electric field at an elevated temperature, and then etched away with a thin layer of oxide. This technique was

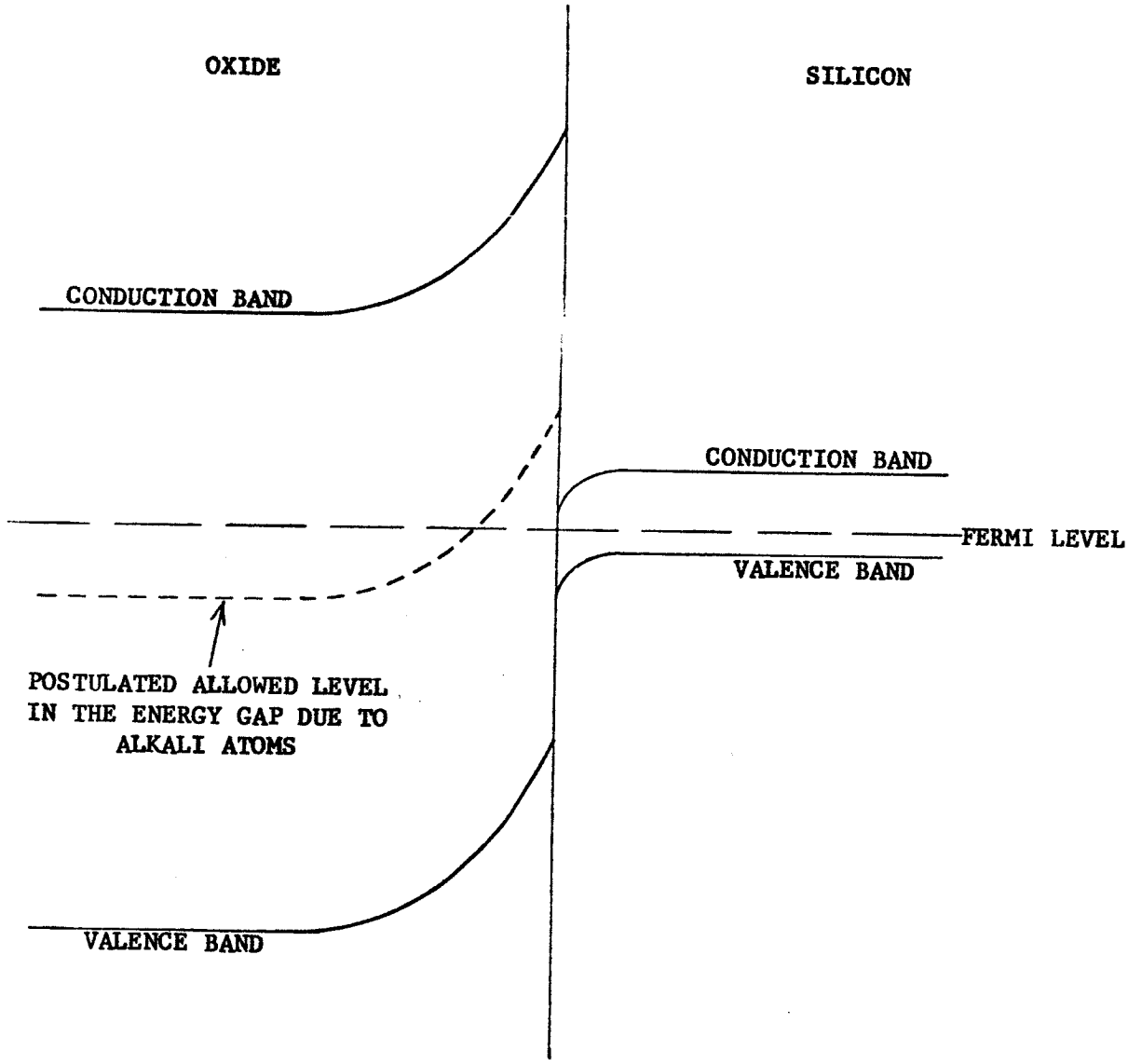


Figure 20. Postulated energy band diagram including a single level due to alkali atoms.

attempted early in this program. The samples were heated to 300°C while an electric field was applied across the oxide by the large-area silicon electrode shown in Figure 13. Following the drifting process, a thin layer of oxide was removed by etching. Alternatively, some oxides were metalized with evaporated aluminum and heated under bias, after which the aluminum and a thin layer of oxide were etched away. Some ions were removed, but a substantial number remained. In view of the fact that the sodium is only partially ionized, one would have to drift and etch away ions repeatedly to remove most of the sodium. Each step might remove all of the ionized sodium, but then with time the unionized sodium would again gradually equilibrate to an ionized state. Smaller and smaller amounts would be taken out in each subsequent step.

3.3 Results of Efforts to Prepare Alkali-Ion-Free Oxides

Practical techniques have been developed that successfully prevent alkali ions from contaminating the oxide during the fabrication processes of MOS devices. These techniques are similar to those developed by Fairchild Semiconductor for their Planar II process and Philco has a license agreement for the use of the techniques. The present process of Philco involves the careful control of material, equipment, and procedures to eliminate, as far as practical, all possible sources of alkali ion contamination. This control extends from the silicon wafer cleaning and etching, through oxidation, metalization, photolithography, alloying, gettering, mounting, and packaging. Further details appear in References 254 and 255.

The degree to which we have been able to produce MOS capacitors with a minimum amount of instability due to alkali ions in phosphorus free oxides is reported in Tables B-1 and B-2 in Appendix B. These data show that the density of mobile alkali ions has been held below 1×10^{11} alkali ions/cm^2 in most thermally grown oxides or vapor plated oxides made with CO_2. Typical levels were about 5×10^{10} ions/cm^2. The data indicate that a level of 1×10^{10} ions/cm^2 is attainable.

Table B-3 of Appendix B contains a tabulation of the mobile ion densities formed in transistors fabricated in this program. Group 217 is a group of p-channel transistors made with an oxide that was thermally grown at 1200°C on ⟨111⟩ oriented silicon, phosphorus-doped to 1.5Ω-cm. The average alkali ion density is 5.7×10^{10} cm^2.

Groups 210 and 213 are p-channel transistors made with an oxide thermally grown at 1200°C on ⟨100⟩ oriented silicon, antimony-doped to ≈ 6.5 Ω-cm. These groups have average alkali ion densities of 2.3×10^{10} and 1.1×10^{11} cm^2. The RT ion and trapping densities in these groups were both less than 10^{10} cm^2.

Table B-4 in Appendix B shows that, of the additional processing steps required to fabricate transistors that are not required for the fabrication of capacitors, the diffusion process was the only one that introduced mobile ions. We believe that alkali ions were introduced by contaminated water used to prepare wet oxygen for growing a layer of oxide during the diffusant drive-in step. This water was contained in a Pyrex (which contains sodium) round bottom flask. The stable MOS transistors described in Table B-3 were made without wet oxidation.

The vapor plated oxides made with SiH_4 were found to have relatively high densities of alkali ions. The reason for the presence of these ions has not been identified, but we believe that with further effort such oxides could be made in stable form.

3.4 Room-Temperature-Mobile Ions (RT Ions)

Hofstein[88,89] has described in detail an instability that exists at room temperature, after a device has been exposed to higher temperatures under a positive bias (on the metal), which is due to some species of highly mobile ion. He has postulated that these ions are protons formed by hydrolysis of water at the metal-oxide interface in the presence of some unknown catalytic agent. He has shown that this instability results from immersing the oxide in hot (90°C) distilled water for 15 minutes, or exposing it to an atmosphere of 60% relative humidity for one hour before metalization. No significant difference was observed among gold, Nichrome, chromium, nickel, and aluminum. The removal of 200 Å of oxide with an $HF-H_2O$ etch before metalization causes devices to be even more stable than the control oxides even though this etching was followed by a water rinse. Hofstein has postulated that the action of the water that produced the instability in the unetched oxide is dependent on the presence of a catalytic agent which is removed when the oxide surface is etched.

Alternatively, the etching operation may leave some residue on the surface that affects the formation of ions in subsequent processing or heat treatments. Gregor[63] very recently reported that the instability is dependent on whether the solvent chemical treatment of the oxide immediately prior to metalization (in his case aluminum) is basic or acidic. He found that nonbasic solvents (Freon, xylene, trichloroethylene, and acidified water) yield a relatively low level of instability, whereas basic solvents (methanol, ethanol, isopropanol, pyridine) cause a large amount of instability. The degree to which these results were due to alkali ions is not clear.

Meyer[152] has shown that silicon oxide surfaces retain a high concentration (10^{17} to 10^{19} atoms per cm^2) of fluorine even after treatments intended to reduce the fluorine concentration. His work shows that very high concentrations are involved and that they are hard to remove. This work supports our opinion that difficult as it is to form clean surfaces it is even more difficult to clean a contaminated surface.

No adequate model for "proton" instability exists. It appears that the phenomenon may be a complex reaction involving various constituents in undefined roles of reactant or catalytic agent. It has been reported[58] that the diffusion of protons or "water" is much more rapid in silica containing aluminum than in pure silica. Hetherington et al[79] state that hydroxyl produced by reaction of vitreous silica with either water vapor of hydrogen can be removed by treatment in vacuum at high temperature. (Burkhardt[265] found that oxides prepared in tritiated steam could be baked at the oxidation temperature in dry O_2 to remove all traces of tritium.) Hetherington et al[79] found that hydroxyl introduced by electrolysis could not be removed by treatment in vacuum at high temperature. They mention that sodium in glass can be replaced by hydrogen in the form of Si-OH groups in electrolysis while in other work hydrogen introduced into glass by electrolysis exists as hydroxyls which are not replaceable by sodium atoms in subsequent electrolysis.

Lee[121] has reviewed the literature on the diffusion of hydrogen and water in fused silica. His work shows the diffusion to be a complex function of temperature, the state of reduction and of the material purity. His model makes a distinction between metastable and permanent hydroxyl.

Much work has been done to study the behavior of water and hydrogen in silica and in MOS oxides. The behavior is complicated. Fortunately, it has been possible to develop practical empirical techniques by which the beneficial effects of water on MOS structures are utilized and it has been possible to fabricate MOS structures without the objectionable RT ion or alkali ion instability.

3.5 Results of Efforts to Prepare Oxides Free of RT Ions

The data in Tables B-1, B-2 and B-3 in Appendix B show that we have been able to keep the density of the charges responsible for RT ion instability down below 5×10^{10} cm^2 most of the time, with many samples having a RT ion density below 1×10^{10} cm^2.

The source of the RT ion instability has not been clearly identified. In some cases, heating the metalized oxide to 475 or 550° C for 5 minutes in dry N_2 increases the instability. In other cases it does not.

The dryness of the oxide does not seem to be an important factor in determining the RT ion instability. The data in Table B-5 in Appendix B seems to show that drier oxides have less RT ion instability; on the other hand, Table B-1 in Appendix B shows that many oxides that were less dry exhibit low levels of RT ion instability.

Rinses or etches in 10:1 HF, buffered HF or deionized water do not always cause RT ion instability.

There appears to be a slightly higher tendency for buffered HF to introduce RT ion instability than for 10:1 HF to introduce RT ion instability.

We found that a methanol rinse before metalization introduced a high level of both alkali ion and RT ion instability, supporting observations by Gregor[65]. It is our understanding that the instability found by Gregor can be interpreted to be due to alkali ions. We believe alcohols contain relatively high levels of sodium contamination.

There appears to be a weak positive correlation between the observed densities of alkali ions and RT ions.

3.6 Phosphosilicate Glass

A deposit of phosphosilicate glass is widely used to produce stabilized MOS devices. Yon et al[250] have shown that sodium is gettered by the phosphosilicate layer. The fact that this layer acts as a barrier has been confirmed by Snow and Deal[209]. They show, however, that if the phosphosilicate glass is too thick relative to the thickness of the underlying pure SiO_2, the pure phosphosilicate glass will itself contribute to an instability because of polarization in the phosphosilicate glass.

The effect of this polarizability can be minimized by making the layer of phosphosilicate glass sufficiently thin so that the polarizable layer has very little effect on the polarization of the total oxide layer. Since this layer is not near the silicon, the effect on the silicon can be quite small. On the other hand, since phosphorus glass is hygroscopic it may be expected to increase the problem of mobile ions on the surface of the oxide.

Phosphorus glass has a higher etch rate than does silicon oxide; therefore, more refined techniques are necessary to form sharply defined cuts in the oxide.

3.7 Model for Instability Due to Slow Traps

Assume that trapping levels exist in the energy gap of the oxide. These traps might be donor (neutral when filled and positively charged when empty) or acceptor (negatively charged when filled and neutral when empty) in the model.

When a negative gate voltage is applied, the potential energy for electrons at the trap sites in the oxide is increased. This increases the probability that the traps are empty, thereby increasing the positive charge in the oxide.

In contrast to the mobile-ion-caused instability described in Figure 19 in which the effective positive charge in the oxide near the silicon is increased by a positive voltage on the metal, trapping-caused instability increases the positive charge in the oxide when there is a negative voltage on the metal. The direction of the instability due to trapping is therefore opposite to that shown in Figure 19.

The presence of slow trapping states was found to be at least partially dependent on the treatment given the silicon surface in preparation for oxidation. Oxides were thermally grown at 1200°C in dry O_2 on wafers having two different kinds of final etching. Wafers that were etched in an acid solution (HF, HNO_3, and HAc) at room temperature exhibited the trapping type of instability in the unmetalized oxide, whereas similar wafers etched at 1200°C in gaseous HCl exhibited some mobile ion instability in the unmetalized oxide. Rinsing was not required following the gaseous etching. An experiment showed that samples rinsed after gaseous etching did not exhibit trapping, indicating that the difference was due to the method of etching and not due to the rinsing. The same results were found in metalized vapor-plated silicon nitride layers on silicon prepared with gaseous or liquid etching.

3.8 Coexistence of Trapping and Mobile Ion Instability

Trapping and mobile charge coexist in at least some samples. This can be shown by performing the drift testing under various conditions of applied bias and temperature. If sufficient time is allowed for the mobile charge motion to saturate and if a sufficient bias voltage is applied to prevent the mobile charge from rearranging itself to reduce the field in the oxide to zero, then the mobile charge should drift in the oxide to a saturation point which is independent of the applied voltage. On the other hand, the trapped charge would be sensitive to the applied voltage because the occupancy of a trap depends on the electrostatic potential at the trap site. The occupancy of the trap depends also on the temperature because of the influence of the temperature on the Fermi level.

To demonstrate the coexistence of mobile charge and trapped charge, measurements were made on packaged capacitors made with vapor plated nitrides with aluminum metalization. These samples, which were made on another program, were chosen for this experiment because they exhibited more trapping than any of our oxide samples. To measure the instability a negative voltage of the magnitude and at the temperature indicated in Table 1 was applied for 15 minutes to the metal electrode. The inflection voltage of the C-V curve was measured. Following this a positive voltage of the same magnitude was applied to the metal electrode at the same temperature, again for 15 minutes. The inflection voltage of the C-V

TABLE 1

DEMONSTRATION OF COEXISTENCE
OF MOBILE CHARGE AND TRAPPED CHARGE

TEMPERATURE		BIAS	MAGNITUDE & TYPE OF INSTABILITY	
DRIFT	TEST	VOLTAGE	SAMPLE #1	SAMPLE #2
22°C	22°C	2 V	12 V mobile ion	2 V trapping
"	"	12 V	2 V trapping	6 V trapping
"	"	50 V	7 V trapping	20 V trapping
22°C	-78°C	2 V	2 V trapping	0 V
"	"	12 V	1 V trapping	0 V
"	"	50 V	20 V trapping	10 V trapping
-78°C	-78°C	2 V	5 V trapping	3 V mobile ion
"	"	12 V	2 V mobile ion	2 V mobile ion
"	"	50 V	0 V	4 V trapping

curve was measured again. The magnitude of the instability recorded in Table 1 is the difference between these two readings and the instability type (mobile ion or trapping) was determined by the direction of the shift of the C-V curve during the second drift operation.

The results in Table 1 show that it is possible to vary the drift voltage to influence the relative amount of trapping. More trapping is observed, the higher the drift voltage. Decreasing the temperature appears to decrease the trapping instability more than it does the mobile ion instability.

In summary, it should be recognized that trapping and mobile ion instability can coexist and can compensate for each other, and it appears that the technique, for which we have shown feasibility, can be developed into a practical method for studying the relative magnitudes of these types of instability.

3.9 Observed Levels of Trapping Instability

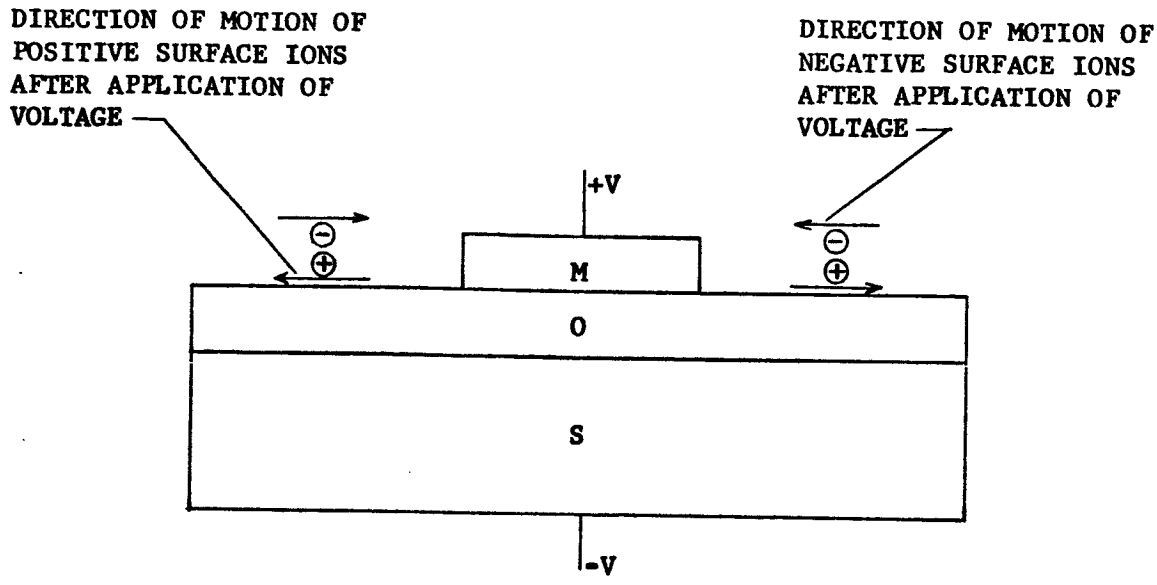
The data in Tables B-1 and B-2 in Appendix B show that trapping is not a serious cause of instability in thermally grown oxides. Trapping appears to be more of a problem in vapor plated oxides. Vapor plated oxides made with CO_2 have 1.0×10^{10} to 4.0×10^{10} trapped charges/cm^2. Vapor plated oxides made with SiH_4 have 0.3×10^{11} to 2.0×10^{11} trapped charges/cm^2. Vapor plated silicon nitrides were found to have 0.6×10^{11} to 6.0×10^{11} trapped charges/cm^2. Kerr[277] has also reported high trap densities in nitrides.

3.10 Surface Ions

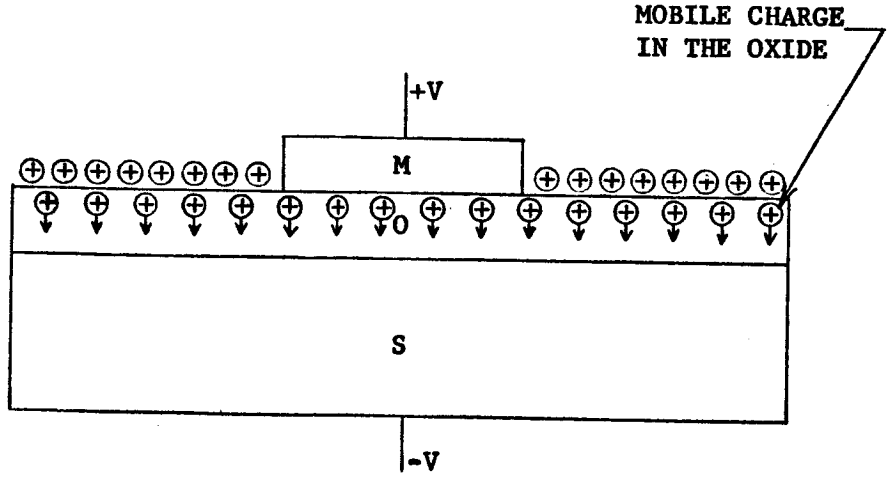
Another cause of microcircuit instability involves the motion of ions along the surface of an oxide. Such ionic motion has been studied by Shockley et al[205,206]. This kind of charge motion can influence the surface potential of the silicon to induce channels or to affect diode characteristics in either bipolar or MOS devices or microcircuits. If there are ions on the surface, the application of a voltage to a metal electrode may influence the electrostatic potential distribution over adjacent unmetalized regions of the oxide surface of the device or circuit. Whereas surface ions alone are quite capable of affecting the surface potential of the silicon, their effect is increased when they cause the movement of mobile ions in the oxide.

Referring to Figure 21, if a positive voltage is applied to the metal, mobile ions on the surface of the oxide will move so as to make the surface potential of the oxide around the metal more positive. This increase in oxide surface potential will cause any positive ions in the oxide to move toward the silicon. This redistribution of charge in the oxide causes the surface potential of the silicon to become more negative. This change in silicon surface potential can create or affect channels and can alter diode characteristics.

Several experiments have been conducted that show these effects. In one experiment, an oxide was prepared to have a high density of sodium ions. It was then formed into MOS capacitors. These were scribed and mounted so as to have two capacitors on one silicon chip mounted in a package. Some of the packages were hermetically sealed while others had an intentional hole in the package. Initially, the C-V curves were recorded for each pair of capacitors. A positive bias of +12 V was then applied to the metal electrode of one capacitor in each package for four days at room temperature while the other capacitor was open circuited. After this, the C-V curves were measured again to determine whether the presence of an applied voltage on the one capacitor could influence the charge and therefore the C-V characteristics of the other capacitor. The results are given in Table 2.



a.



b.

Note: The ionic motion depicted in a. develops a positive electrostatic potential on the oxide surface that causes the mobile charge in the oxide to drift toward the silicon as shown in b.

Figure 21. Model for the effect of mobile surface ions.

TABLE 2

INTERACTION OF TWO CAPACITORS
ON THE SAME SILICON CHIP

Device No.	Capacitor	FLAT BAND VOLTAGE (volts) Initially	After 4 days of +12 V on Capacitor A	
185B1	A	2.6	3.4	Hermetic Package
	B	2.6	2.9	
179A2	A	3.4	5.4	
	B	3.6	4.4	
179A3	A	4.3	10	
	B	3.5	3.9	
179A1	A	3.6	7.5	Leak in Package
	B	3.6	7.5	
179A2	A	3.2	6.6	
	B	3.2	4.9	
185B2	A	2.3	4.4	
	B	2.3	2.8	

TABLE 3

EFFECT OF MOBILE IONS ON THE SURFACE

Sample #	CHANNEL CURRENT (mA) AT 3 V Initial	After 24-Hour Bias Period	
7	0.39	0.40	Hermetic Package
9	0.23	0.23	
10	0.47	0.47	
3	0.36	1.67	Leak in Package
6	0.36	0.40	
8	0.56	2.12	

The data in Table 2 show that a voltage applied to capacitor A influences the distribution of charge in capacitor B. We believe that this indicates that charge motion on the surface of the oxide established a voltage on capacitor B.

It is possible that the charge motion described above may have been through the glass in the package. The following experiment was conducted in which the possible charge motion through the glass of the package could not influence the results. A number of n-channel MOS transistors were mounted and packaged without a whisker connection from the gate to the package. The source-to-drain current was measured at a source-to-drain voltage of 3 V. A positive 20 V was applied to the source and the drain relative to the substrate, for a period of twenty-four hours. Since there was no connection to the gate, the gate potential could only change due to charge motion along the oxide surface from the source and drain bonding pads. Some of the packages were hermetic and some had intentional air leaks in the package. The results are given in Table 3.

We believe that the data in Table 3 clearly demonstrate that ions can move along the top surface of an oxide to alter the characteristics of MOS devices, particularly when packages are not hermetic. We infer from this data that ions on an oxide can alter the surface potential of the underlying silicon at points not covered by a metal layer.

In n-channel MOS transistors, the gate is frequently designed so as not to overlap the drain region in order to reduce the gate-to-drain capacitance. In this case, the negative potential normally found at the silicon surface under oxides make the part of the channel between the gate and the drain conductive.

Assuming the application of a negative voltage to turn off the channel for a long time (hours or days), mobile ions on the oxide surface would move in such a way to make the silicon surface potential less negative. This would reduce the conductivity of the channel between the edge of the gate and the drain. When the voltage on the gate is then made positive, the channel between the edge of the gate and the drain would not have its desirable high conductance, thereby reducing the over-all channel conductance and the transistor transconductance.

Metz[151] and Atalla[6] have shown that mobile surface ions can influence the electric field at the silicon surface at the edge of a p-n junction to influence the diode breakdown voltage and the diode leakage current in bipolar devices.

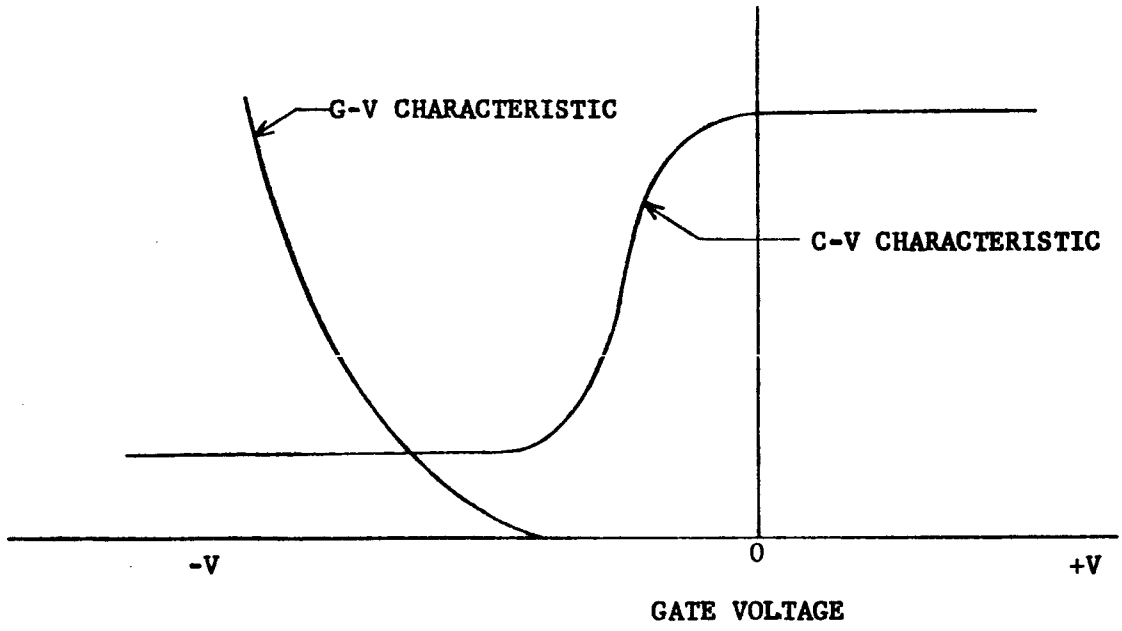
Rosier[194] has described how the surface recombination velocity depends on the surface potential of the silicon. Mobile surface ions cause instability of the beta of bipolar transistors through their effect on surface recombination velocity.

4. THRESHOLD VOLTAGE OF MOS DEVICES

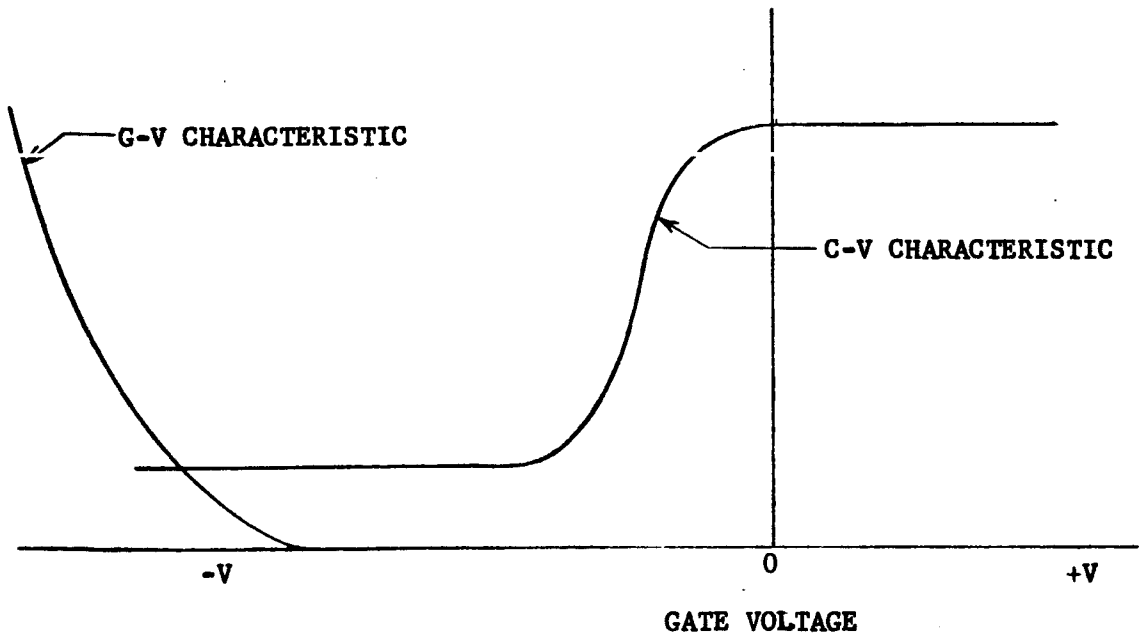
4.1 Effects of Oxide Charge and Traps

The threshold voltage of an MOS transistor is that gate-to-substrate voltage (source connected to substrate) at which the channel between the source and the drain is just at the edge of conduction. In an n-channel MOS transistor, this is the negative voltage which must be applied to the gate to repel the normally occurring inversion layer of electrons so that the normally-on channel is just at the point of being turned off. Similarly, in a p-channel MOS transistor, this is the negative voltage that must be applied to the gate to attract holes to make this normally off channel start to conduct current.

The threshold voltage depends mainly on two parameters: the charge density in the oxide, and the average mobility of induced charges in the channel. The presence of charge in the oxide influences the silicon surface potential and thereby determines the relationship between the applied voltage and the density of net charge in the silicon, as described in subsection 1.5. The conductance of the transistor channel depends not only on the density of charges in the channel region but also on their mobility. Trapped charge is not mobile and therefore does not contribute to the mobility. During the long history of field effect devices, a major problem has been that fast states that trap and immobilize charge carriers exist at many silicon surfaces. Where these traps exist in sufficient abundance, conduction of a channel does not occur when the charges begin to appear but appears only after a sufficient number of charges have been induced first to fill the traps. This can be demonstrated by superimposing capacitance-voltage (C-V) characteristics on conductance-voltage (G-V) characteristics for a given MOS structure. If there are no fast states, the onset of an inversion layer and of channel conduction occur at nearly the same gate voltage, as shown in Figure 22a. If traps are present, the first carriers induced in the inversion layer do not carry current because they are trapped. A higher voltage must be applied to fill the traps before current starts to flow, as shown in Figure 22b.



a.



b.

Figure 22. Effect of traps on the relationship between the capacitance-voltage and the conductance-voltage characteristics.

4.2 Results of Efforts to Reduce the Immobile Charge Density

In the development of techniques to reduce the threshold voltage we first directed attention to the immobile charge density in the oxide. We conducted experiments to find processes for producing oxides with low immobile charge densities in the hope that, having found such processes, they would yield oxides with low trap densities. The degree to which we have been successful is reported in subsection 4.3.

4.2.1 Effect of Silicon Orientation on Immobile Charge Density

The industry has been using ⟨111⟩ oriented silicon for making MOS transistors. Our experiments and those of other investigators reported below have shown that the immobile charge density is very dependent on the silicon orientation.

The data in Tables B-1 and B-2 in Appendix B show that for thermally grown oxides prepared at 1200°C the immobile charge densities are, typically, those shown in Table 4.

TABLE 4

DEPENDENCE OF IMMOBILE CHARGE DENSITY ON SILICON ORIENTATION

Silicon Orientation	Conductivity Type	Immobile Charge Density (charges per cm^2)
⟨111⟩	n	$1.8 - 2.3 \times 10^{11}$
⟨100⟩	n	0.4×10^{11}
⟨111⟩	p	$2.0 - 2.3 \times 10^{11}$
⟨100⟩	p	$2.7 - 3.0 \times 10^{11}$
⟨110⟩	p	$3.6 - 3.8 \times 10^{11}$

This is in agreement with the data reported by Balk et al[9] who found the immobile charge density to have the following dependence on orientation for n-type silicon:

<111>	3×10^{11} cm^{-2}
<110>	1×10^{11} cm^{-2}
<100>	5×10^{10} cm^{-2}

Balk et al[9] stated that they found "similar results" on p-type silicon. Our data summarized in Table 4 shows an orientation dependence for both n- and p-type silicon but not the same dependence.

Miura[154] obtained similar results for n-type silicon:

<111>	1.2×10^{11} cm^{-2}
<211>	4.5×10^{10} cm^{-2}
<110>	2.4×10^{10} cm^{-2}
<100>	-1.2×10^{10} cm^{-2}.

The negative sign indicates that the electron concentration was depleted at the silicon surface.

4.2.2 Lower Immobile Charge Density in Vapor Plated Oxides

We found an alternative approach for producing oxides with low densities of immobile charge. Vapor plated (with CO_2) oxides formed on both <100> and <111> oriented silicon were found to have substantially lower immobile charge densities than did thermally grown oxides on silicon with the same orientations.

As shown in Table B-1 in Appendix B, the immobile charge densities obtained for vapor plated oxides were 0.9×10^{11} to 1.7×10^{11} cm^{-2} for <111> n-type silicon, and -0.3×10^{11} to less than 10^{10} cm^{-2} for <100> n-type silicon.

A vapor plated (CO_2) oxide on <111> p-type silicon (not shown in Table B-1 because it had a very high mobile ion content) had an immobile charge density of 2.0×10^{11} to 2.7×10^{11} cm^{-2}.

Table B-1 shows that a vapor plated oxide (Sample #190) made with phosphorus doping in the oxide on ⟨111⟩ n-type silicon had an immobile charge density of 2.7×10^{11} to 3.2×10^{11} cm^{-2}.

As Table B-1 further shows, oxides vapor plated with SiH_4 did not show an immobile charge content below that for thermal oxides on either ⟨111⟩ or ⟨100⟩ n-type silicon.

Although others have reported studying vapor plated oxides, the reports give no indication that lower immobile charge densities were found. Very recently, Tarui et al[281] reported that vapor plated oxides made with CO_2 were found to have oxide charge densities that were not significantly different from the densities found in their thermally grown oxides. They found that the magnitude of these charge densities was determined by the post deposition treatment of the oxide. They suggest that the source of this charge density is the SiO_2 surface rather than the oxide silicon interface. It may be that much of the charge in their oxides was mobile. Their observations that a P_2O_5 treatment always yielded a lower charge density might indicate that the mobile charge was gettered. They further reported that their vapor plated oxides had lower densities of surface states (called traps in this report) than their thermally grown oxides.

4.2.3 Effect of Oxidation Temperature on Immobile Charge Density

Another way in which the immobile charge density has been reduced has been to prepare the thermal oxides at lower temperature. Oxides grown at 1200°C typically contain 2.0×10^{11} to 2.4×10^{11} immobile charges/cm^2. Oxides grown at 1000°C were found to have 1.3×10^{11} to 1.5×10^{11} immobile charges/cm^2 and those grown at 900°C have 1.9×10^{11} to 2.2×10^{11} immobile charges/cm^2.

Deal et al[263] have recently reported that the immobile charge density of thermally grown oxides increases with lower oxidation or heat treatment temperatures over the range of 600 to 1200°C. This effect was found to be more pronounced for dry oxidations than for wet oxidations. Our finding of a lower immobile charge density for lower oxidation temperatures appears to contradict the results reported by Deal et al. Possibly there are several competing influences involved to cause our results over the temperature range of 900°C to 1200°C to differ from those obtained by Deal et al over the range of 600 to 1200°C. We did find a higher density for 900°C (1.9×10^{11} to 2.2×10^{11} cm^{-2}) than for 1000°C (1.3×10^{11} to 1.5×10^{11} cm^{-2}). It is our impression that the charge density at 900° to 1000°C reported by Deal et al was about a factor of 2 to 3 higher than ours. It may be that the density of immobile charge

is influenced by stresses due to the difference between the coefficients of thermal expansion of the silicon and of the oxide. The cooling schedule may also influence the immobile charge density. Our cooling schedule is described in subsection 6.6.

4.2.4 Effect of Oxygen Dilution During Oxidation on Immobile Charge Density

As stated in paragraph 4.2.3, above, we found that a reduction in oxidation rate obtained by a reduction in the thermal oxidation temperature, decreases the immobile charge density. In contrast to this we found (Sample #125 in Table B-1 of Appendix B) that a thermal oxide prepared on ⟨111⟩ n-type silicon in 1% dry O_2 and 99% dry N_2 at 1200° C has an immobile charge density of 3.6×10^{11} to 3.9×10^{11} cm^{-2}.

4.2.5 Effect of Nickel or Gold on Immobile Charge Density

We found that the immobile charge density can be reduced in thermally grown oxides by a treatment involving nickel. Electroless nickel is plated on the back face of the silicon. This plating step is followed by a heat treatment in dry N_2. The samples were cooled quickly after the heat treatment. Our findings are summarized in Table 5.

TABLE 5

RESULTS OF TREATMENT INVOLVING NICKEL

Heat Treatment Temperature and Time		Immobile Charge Density (cm^{-2})
1200° C	20 minutes	0.5 to 1.6 x 10^{11}
1050° C	40 minutes	1.6 x 10^{11}
900° C	40 minutes	0.9 to 1.1 x 10^{11}
Control samples		1.9 to 2.3 x 10^{11}

Dunavan and Lawrence[41] found that gold doping of the silicon caused a shift from an n-type surface potential to a strong p-type surface potential.

4.2.6 Effect of Post-Oxidation Heat Treatments on Immobile Charge Density

Figure 23 summarizes experimental data taken in this program showing that heat treatments can be used to change the density of immobile charges of thermally grown oxides. A 300°C bake for 1 hour reduces the immobile charge density by about 20%. These data were taken early in the program. The values plotted are the points of inflection in the C-V curves. The reduction in immobile charge density during a heat treatment at 300°C was found in the driest oxides that we made and tested, indicating that the reduction does not depend on water. Heat treatments at 300°C in dry N_2 for 1 hour do not appear to reduce the charge density in the oxides prepared by vapor plating with CO_2. The charge in such oxides is increased by a factor of 4 by a heat treatment at 450°C for 1 hour in room air.

We have recently prepared very dry oxides grown thermally at 1200°C on both ⟨111⟩ and ⟨100⟩ n-type silicon. We measured the charge density in these samples with a gold ball probe before and after a bake in H_2 for 1 hour at 450°C. This treatment increased the charge density as shown in Table 6.

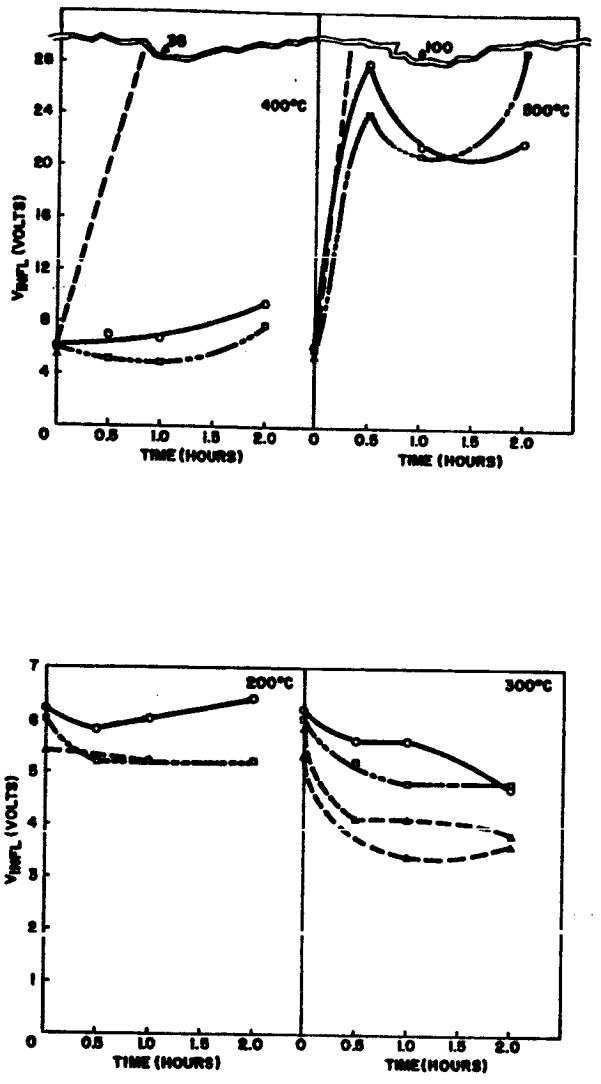
TABLE 6

EFFECTS OF 1-HOUR BAKE IN H_2 AT 450°C
ON THE CHARGE DENSITY OF UNMETALIZED OXIDES

Silicon Orientation	Charge Density	
	Initial	After Bake
⟨111⟩	3×10^{11} cm^{-2}	13×10^{11} cm^{-2}
⟨100⟩	1×10^{11} cm^{-2}	$4\text{-}10 \times 10^{11}$ cm^{-2}

In subsection 6.3, we show that heat treatments in water-containing ambients in the temperature range of 400-1200°C also produce large increases in the immobile charge density in both thermally grown and vapor plated oxides.

In a related company-sponsored program, we found that the threshold voltage of n-channel MOS transistors was increased by such treatments. The silicon was 10 Ω-cm p-type, oriented on the ⟨111⟩ planes. The heat treatment chosen to increase the immobile charge density was 500°C in room air (50% relative humidity at 25°C)



LEGEND

He AMBIENT (DRY)

N_2 AMBIENT (DRY)

AIR AMBIENT (ROOM)

0.3 μ SiO_2

Figure 23. Effects of heat treatment.

for 1 hour. These transistors had a threshold voltage of -6 to -7 volts. The control group which was processed identically except for the 500°C heat treatment had a threshold voltage of -1 volt.

We note that Kooi reports finding a reduction in the immobile charge density due to a heat treatment at 450°C for 30 minutes in wet N_2 (N_2 bubbled through water at room temperature) or wet O_2.

4.3 Results of Efforts to Fabricate Transistors with Lower Threshold Voltage

Having established several techniques by which the immobile charge density in oxides can be reduced in MOS capacitor structures, we made MOS transistors to determine the compatibility of these techniques with transistor fabrication processes and to determine the degree to which fast states or trapping influences the threshold voltage in such transistors.

4.3.1 Thermally Grown Oxides on ⟨100⟩ and ⟨111⟩ Oriented Silicon

Two groups of p-channel MOS transistors were made on antimony-doped 6.7 ohm-cm silicon oriented on the ⟨100⟩ planes. The oxide was thermally grown at 1200°C. The data for each of a group of individual transistors is given in Table B-3 in Appendix B.

The data show that the use of ⟨100⟩ silicon instead of ⟨111⟩ silicon (both with thermally grown oxide) reduces the threshold voltage. The ⟨111⟩ group had an average threshold voltage of 5.9 V and the two ⟨100⟩ groups had average threshold voltages of 1.2 and 2.0 V.

The stability of these transistors is demonstrated by the low mobile ion densities shown in Table B-3. Leakage currents were measured on these transistors at a drain-to-substrate voltage of -4 V. Most of the leakage currents of the drain-substrate diodes in the transistors made on ⟨100⟩ silicon were in the range of 0.01 to 0.10 nanoamperes. This is at least as low as that in similar devices on ⟨111⟩ silicon.

4.3.2 Vapor Plated Oxides on ⟨100⟩ and ⟨111⟩ Oriented Silicon

We made p-channel MOS transistors with a vapor plated oxide on phosphorus doped silicon oriented on the ⟨111⟩ and on the ⟨100⟩

planes. The drift testing sequence described in subsection 2.6 showed a slow trap density of $\approx 7 \times 10^{10}$ cm^{-2}. The threshold voltages of these transistors were 4 to 5 V on the ⟨100⟩ silicon and 5 to 7 V on the ⟨111⟩ silicon. C-V measurements, gate to substrate, indicate that this high threshold voltage was partially due to a relatively high immobile charge density and partially due to trapping. The processing of these transistors included the formation of a thermally grown oxide which served as the diffusion mask. After the diffusion of the source and drain regions the thermally grown oxide was etched away in the gate region and a vapor plated oxide was deposited. We postulated that the oxide etching operation left a surface which, after the subsequent deposition of a vapor plated oxide, had a high density of immobile charge. Additional transistors were made on ⟨111⟩silicon, but in this case the oxide etching operation was followed by another etch which removed a thin layer of silicon. In these transistors the threshold voltage was again 6 to 7 V. More work will be necessary to determine the feasibility of making MOS transistors having low threshold voltages with vapor plated oxides. The recently published report by Tarui et al[281] in which they found low trap densities in vapor plated oxides, is encouraging. We are optimistic that further development work will show that vapor plated oxides can be used to make transistors with lower threshold voltages.

5. RADIATION INDUCED DEGRADATION

5.1 Introduction

Experiments conducted in various laboratories show MOS transistors to be sensitive to doses of ionizing (X or gamma) radiation of less than 10^4 rads. In comparison, bipolar transistors can tolerate similar radiation up to approximately 10^6 rads.

Ionizing radiation affects MOS devices to increase the threshold voltage, to decrease the transconductance, and at higher levels to increase the reverse currents of the source and drain junctions. These changes occur because of the development of positive charge in the oxide and because of the development of surface states which trap or immobilize carriers in the channel region of the transistor.

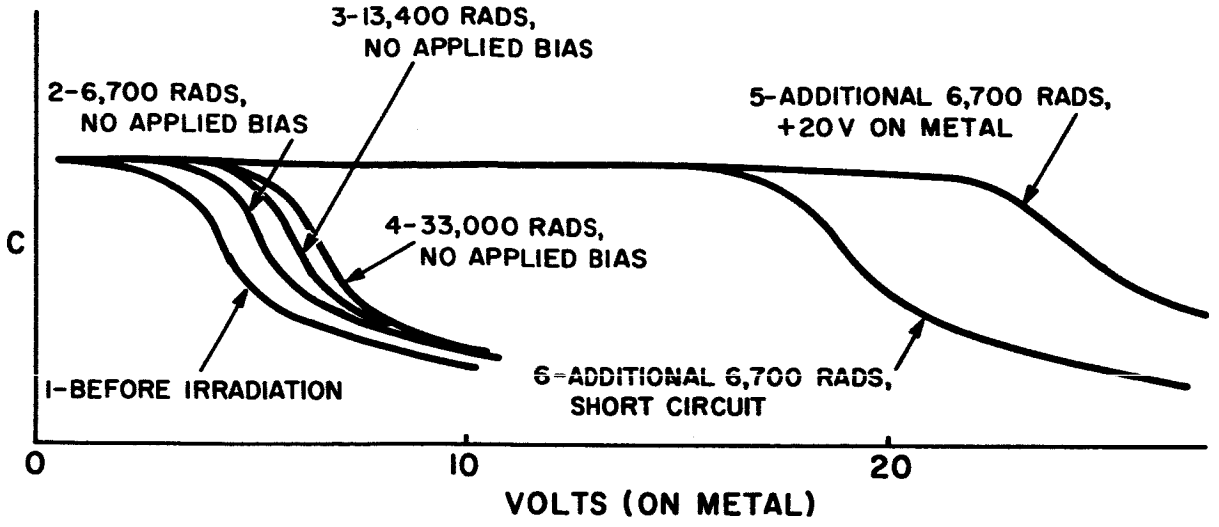
Figure 24 shows some C-V curves that were taken on MOS capacitors after various conditions of exposure to radiation during this program; they illustrate some of the typical behavior of MOS capacitors in ionizing radiation:

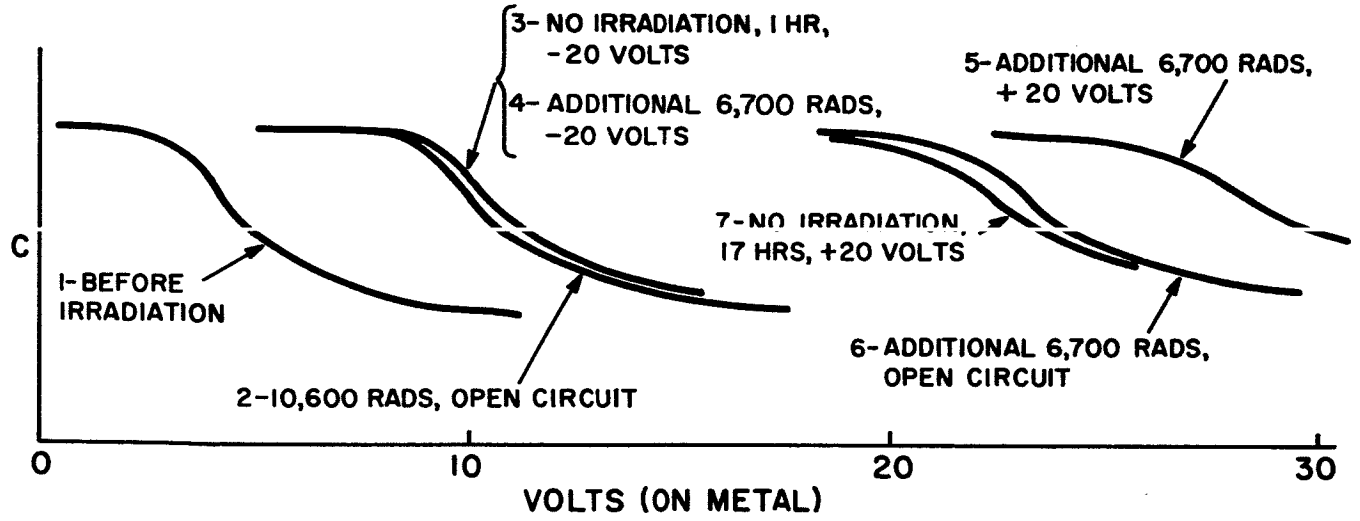
1. The magnitude of the applied negative voltage has little effect on the charge developed in the oxide.

2. The magnitude of the applied positive voltage has a strong effect on the charge developed in the oxide.

3. Degradation under positive voltage is much greater than that under a negative voltage.

4. Continued irradiation with zero or negative applied voltage after an irradiation with a positive applied voltage "anneals" out some of the "damage".





Note: The numerals associated with the curves indicate the order of the testing sequence.

Figure 24. Typical effects of radiation on MOS capacitors.

5.2 Model for Radiation Effect on MOS Devices

Grove* reported that the amount of induced charge during an irradiation with a positive applied voltage saturates at a level proportional to the square root of the voltage. He has developed a model for this behavior in which he assumes a uniform distribution of electron traps in the oxide having a density of 1.7×10^{18} cm^{-2}.

According to Grove's model, the X- or gamma-radiation ionizes the SiO_2 and creates hole-electron pairs. Electrons in donor traps in the oxide fall into empty levels in the valence band of the oxide, leaving positively charged donor traps. The electrons and holes in the conduction and valence bands, respectively, of the oxide can flow to the silicon or the metal. The barriers at the oxide interfaces prevent holes or electrons from flowing into the oxide from the metal or the silicon unless the structure is exposed to energetic radiation.

The probability that a trap will remain empty depends on the electrostatic potential at the location of each trap. During the irradiation there are a sufficient number of electrons in the oxide to fill some of the traps. This presence of electrons allows the empty traps to distribute themselves in the oxide in a way that minimizes the electric fields. This situation is very similar to that of a depletion layer at an abrupt p-n junction between two homogeneous regions.

Figure 25 shows how the charge density and the electrical field distribution in the oxide are affected by the irradiation. Figure 25a depicts the charge distribution and field for a given applied voltage, assuming there is no net charge in the oxide before the irradiation. The charge densities on the two faces of the oxide are equal and opposite, and the field is constant throughout the oxide. The radiation uniformly ionizes the traps in the oxide. Those traps located with an electrostatic potential above a certain level and therefore those to the right of a given plane in the structure in Figure 25 remain ionized, whereas those at locations with lower potential are refilled with electrons induced in the oxide by the radiation. These electrons may come from the ionization of the silicon oxide or they may be ejected from the silicon into the oxide by the radiation. Figure 25b illustrates the situation at an intermediate time and when the situation shown in Figure 25c is reached, the field is zero to the left of a given plane and all of the traps are ionized to the right of this plane.

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* A. S. Grove, presention at the Silicon Interface Specialists Conference, Las Vegas, Nevada, November 15-16, 1965. Also see reference 284.

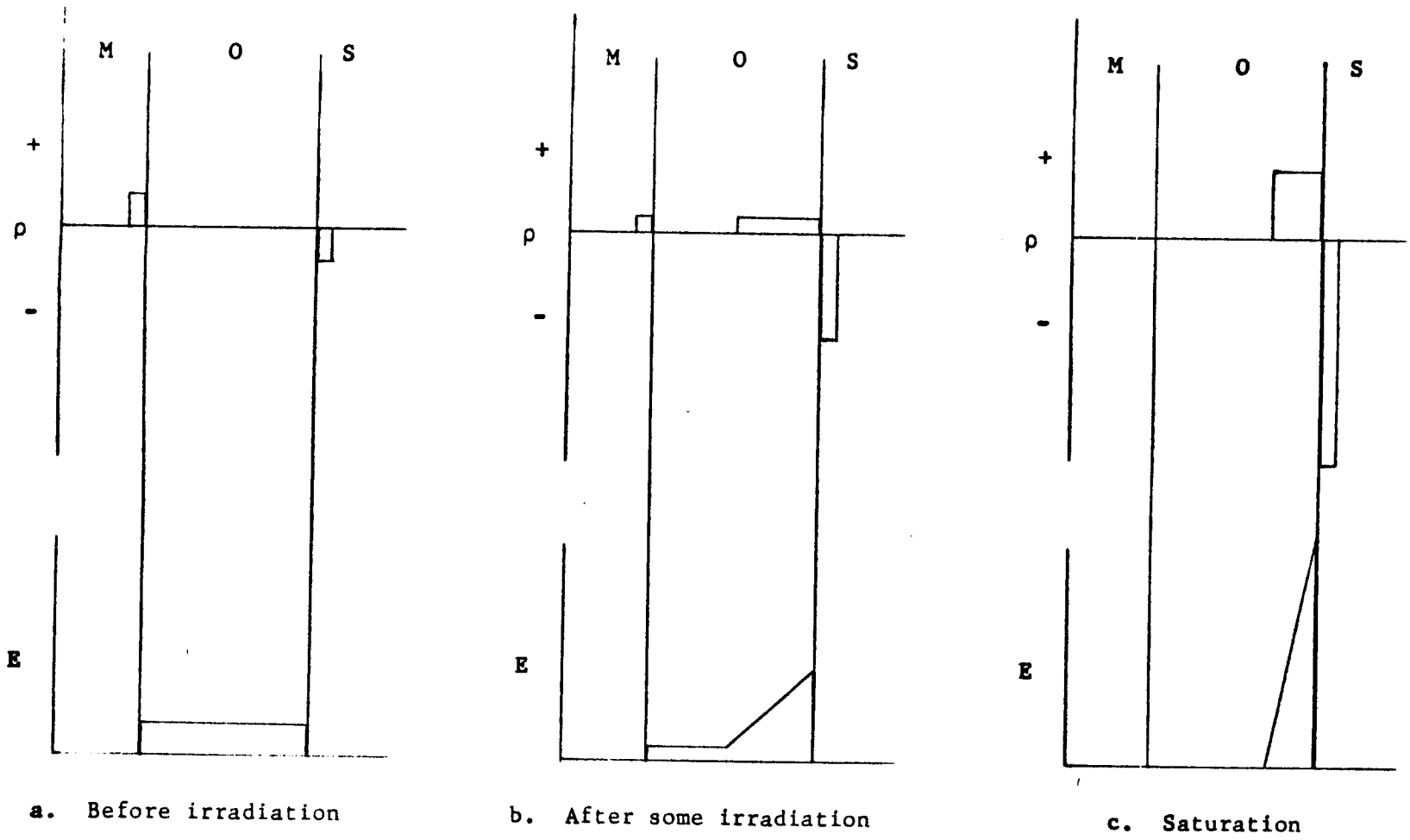


Figure 25. The effect of irradiation on the distributions of charge density (ρ) and electric field (E) in the oxide.

The location of this plane and therefore the number of ionized traps depends on the applied voltage because the probability for occupancy of a trap depends on the potential at the trap site. For a given uniform trap density, the amount of charge contained in traps can be shown to be proportional to the square root of the voltage. (This situation is quite similar to that in which the width of a depletion layer, at p-n junctions between one region of high impurity density and one of relatively low homogeneous impurity density, is proportional to the square root of the applied voltage. For a uniform impurity density, the charge density per unit area is proportional to the square root of the applied voltage.)

After the irradiation, the ionized traps remain positively charged because the conduction band of the oxide is so far above the Fermi level that there are practically no electrons available to neutralize the traps. This radiation induced charge can be annealed out by any means by which electrons can be provided to neutralize the traps. Such means include an increase in temperature or an exposure to ultraviolet light of sufficiently short wavelength. An exposure to X- or gamma-radiation under a negative or zero applied voltage anneals out some of the charge induced during an irradiation under a positive voltage.

Kooi[114] showed that the channel current of n-channel MOS transistors first increases and then decreases during a continuing irradiation. The increase is believed to be due to the ionization of donor traps in the oxide, which induces a higher density of electrons in the inversion layer. The decrease in the channel current with further irradiation is believed to be due to the formation, at the silicon surface, of states which trap carriers and prevent them from contributing to the channel current. The observation that these states are formed in wet oxides and not in dry oxides leads him to believe that they already exist in the silicon under dry oxides before the irradiation.

Kooi has also observed that ultraviolet light decreases the charge more in the wet oxides than in dry oxides. This may be because dry oxides have many more electron traps at the oxide-silicon interface, and therefore fewer electrons can be injected into the oxide from the silicon during the exposure to the ultraviolet light.

5.3 Results of Testing the Radiation Resistance of MOS Devices

Capacitors fabricated by various techniques were irradiated in a Co^{60} source. Figures 26 through 36 show the results.

These figures show the following:

1. Vapor plated oxides degrade very similarly to thermally grown oxides.

2. The radiation resistance of MOS capacitors does not depend on the silicon orientation.

3. Oxides that are practically free of mobile ions degrade similarly to those that contain mobile ions.

4. The radiation resistance is independent of the silicon conductivity type for a given applied voltage. However, because an n-channel MOS transistor would be more likely to be operated with a positive voltage on the gate it would degrade more than a p-channel MOS transistor.

5. Nickel diffusion of the silicon did not affect the radiation resistance.

6. Oxides that were thermally grown at 1000° C were more resistant to radiation than were the oxides similarly grown at 1200° C. (Tables B-1 and B-2 in Appendix B show oxide preparation temperatures for all groups.)

7. Within each group of capacitors there is a positive correlation between the amount of radiation-induced charge and the charge in the oxide at the beginning of the irradiation. That is, the devices which had the highest initial charge density showed the greatest charge density increase due to radiation.

8. Increasing the dryness of oxides by the means described in this report did not significantly affect the radiation resistance of MOS capacitors.

Capacitors made with silicon nitride show much more resistance to radiation than do those made with oxides. In some cases, irradiation of nitride capacitors resulted in a decrease in the net positive charge in the nitride layer. Stanley and Wegener[275] recently reported the superiority of silicon nitride over silicon oxide in electron irradiation. Szedon et al[271] have recently

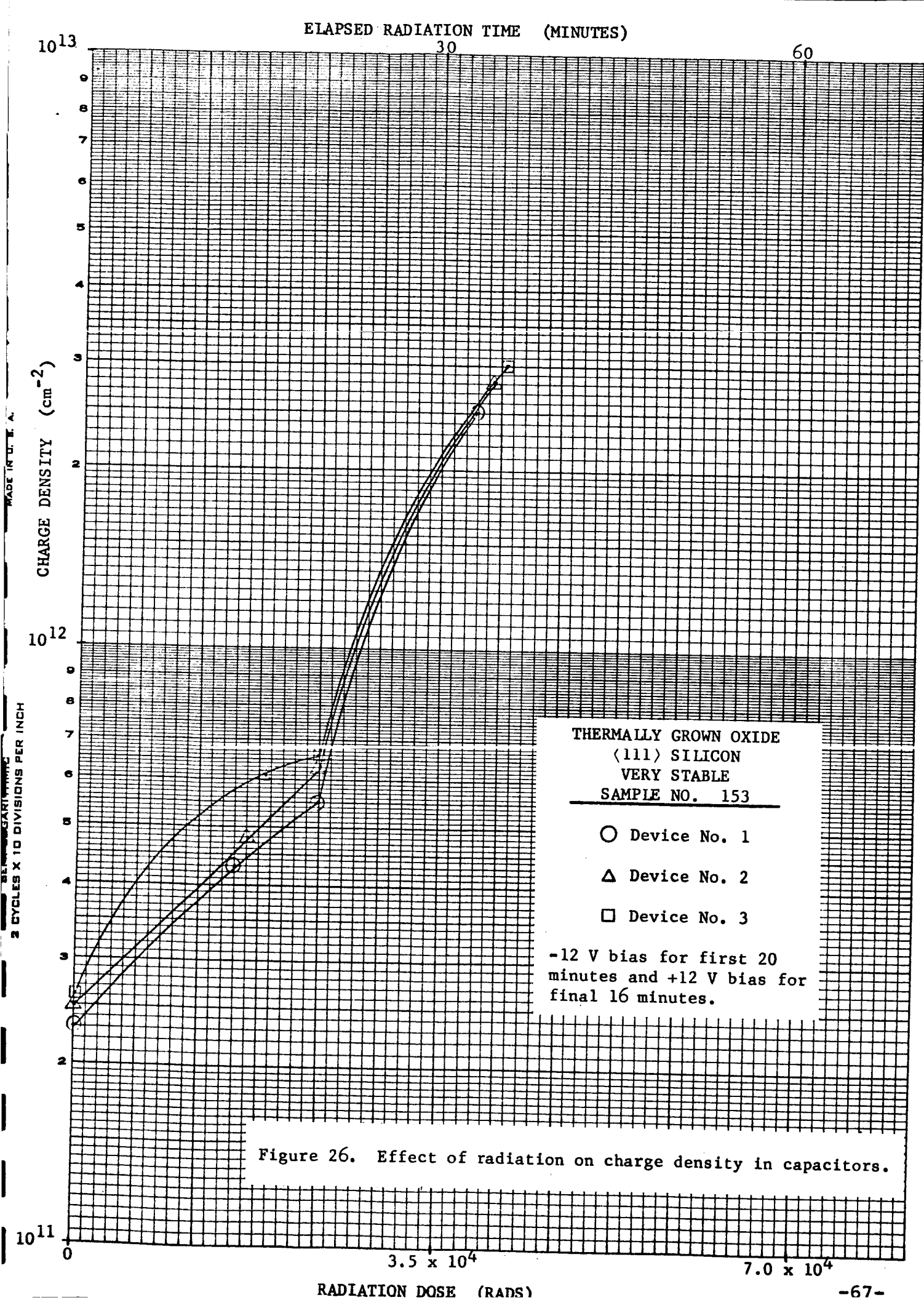


Figure 26. Effect of radiation on charge density in capacitors.

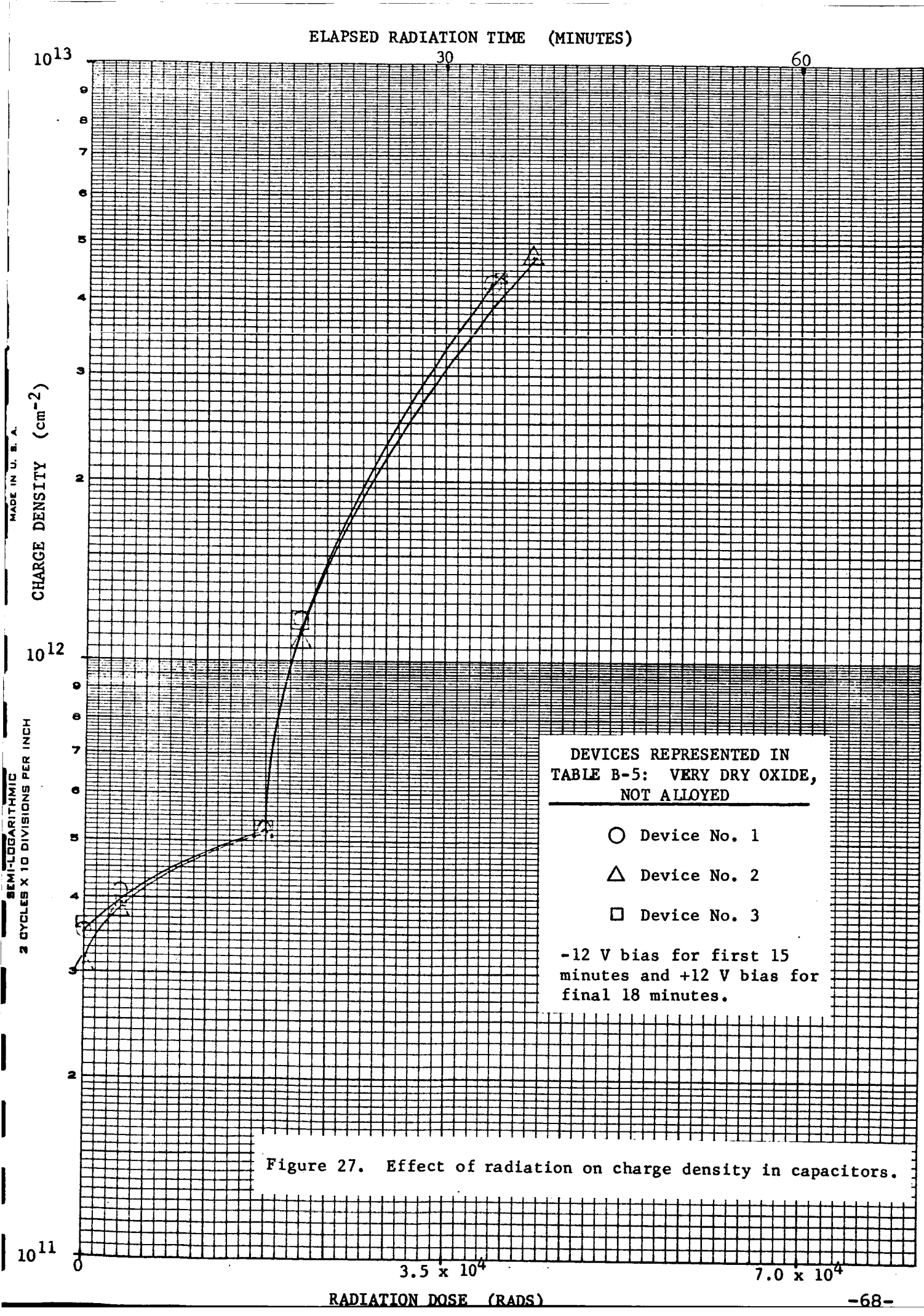


Figure 27. Effect of radiation on charge density in capacitors.

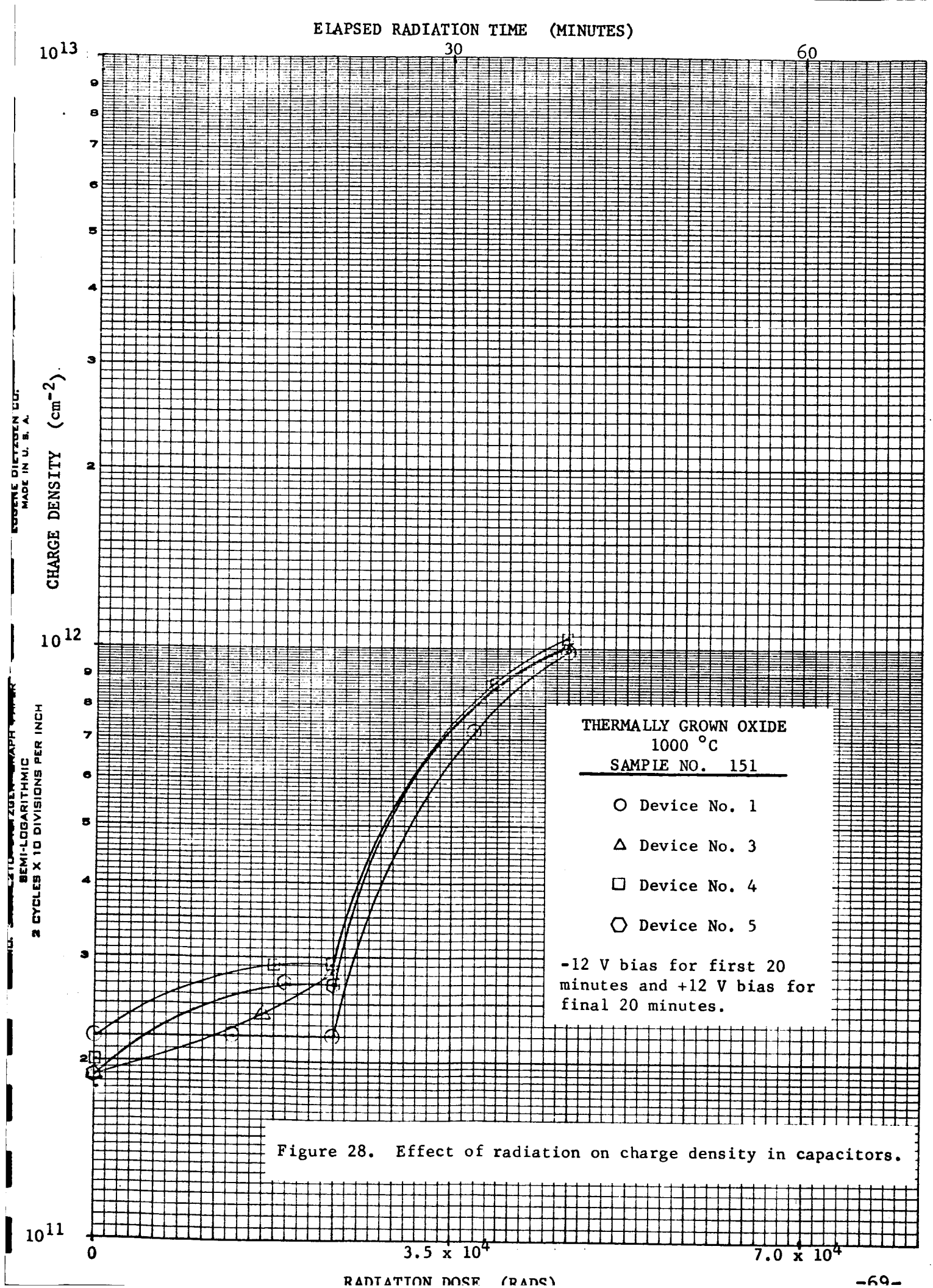


Figure 28. Effect of radiation on charge density in capacitors.

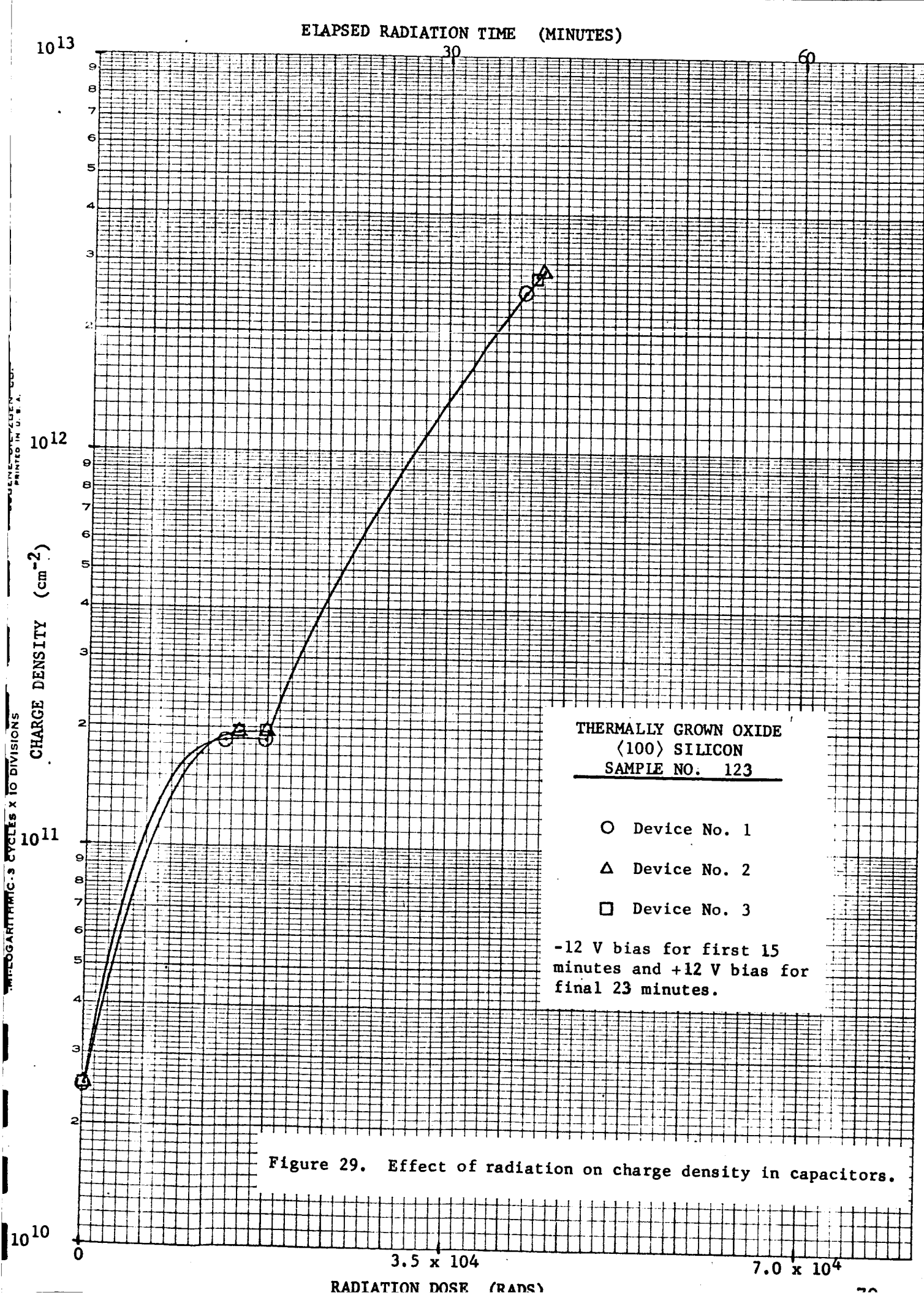


Figure 29. Effect of radiation on charge density in capacitors.

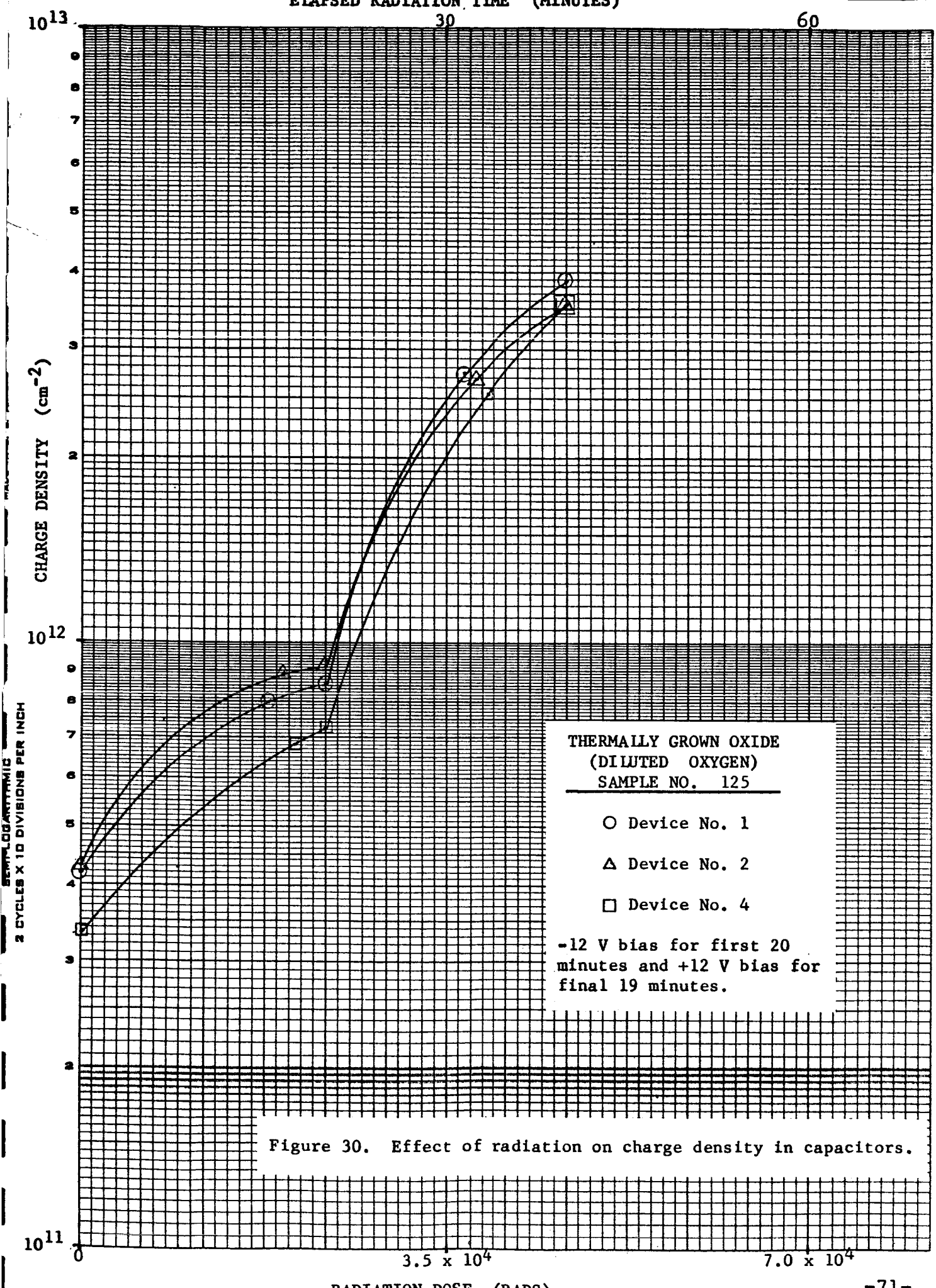


Figure 30. Effect of radiation on charge density in capacitors.

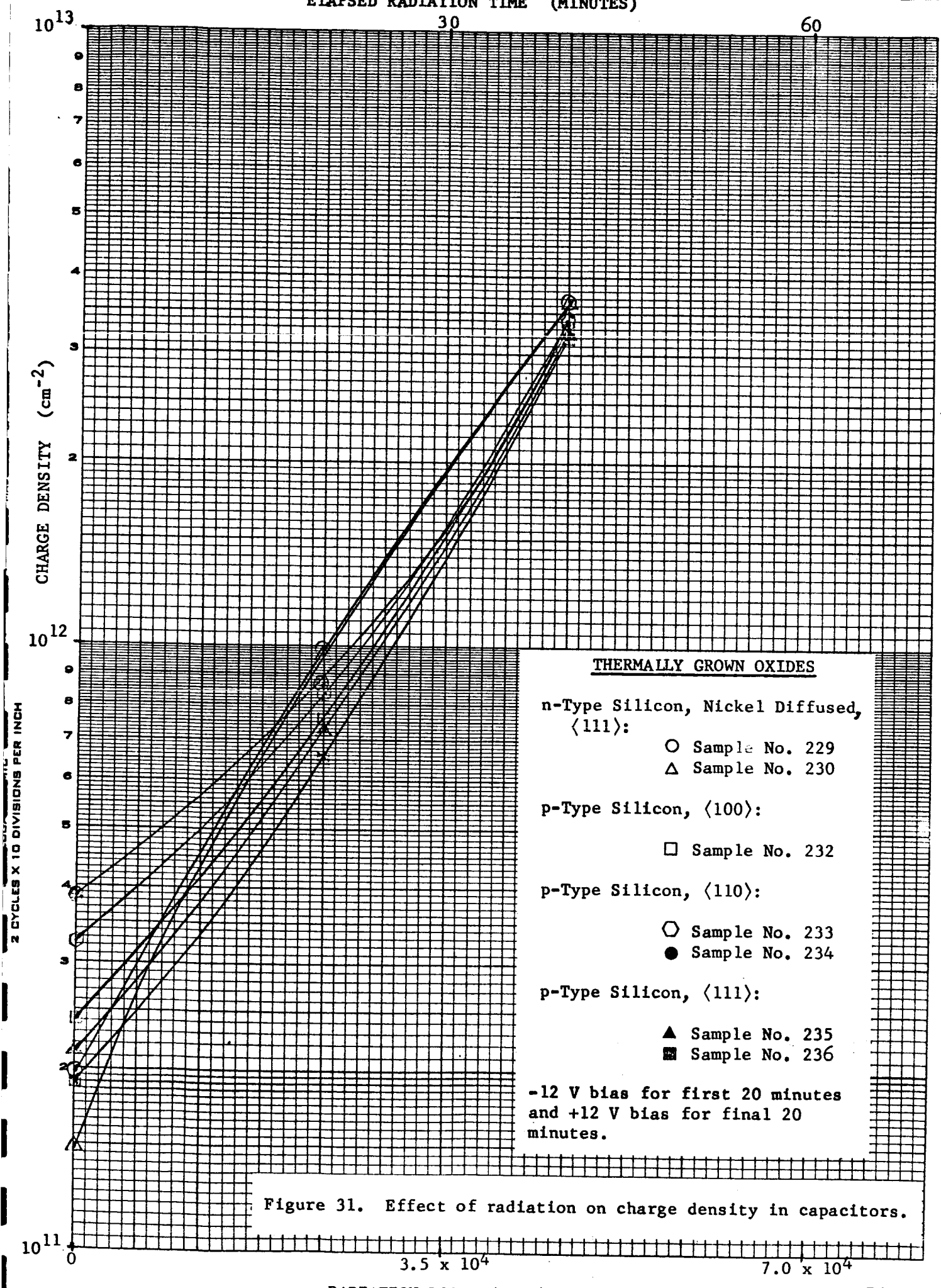


Figure 31. Effect of radiation on charge density in capacitors.

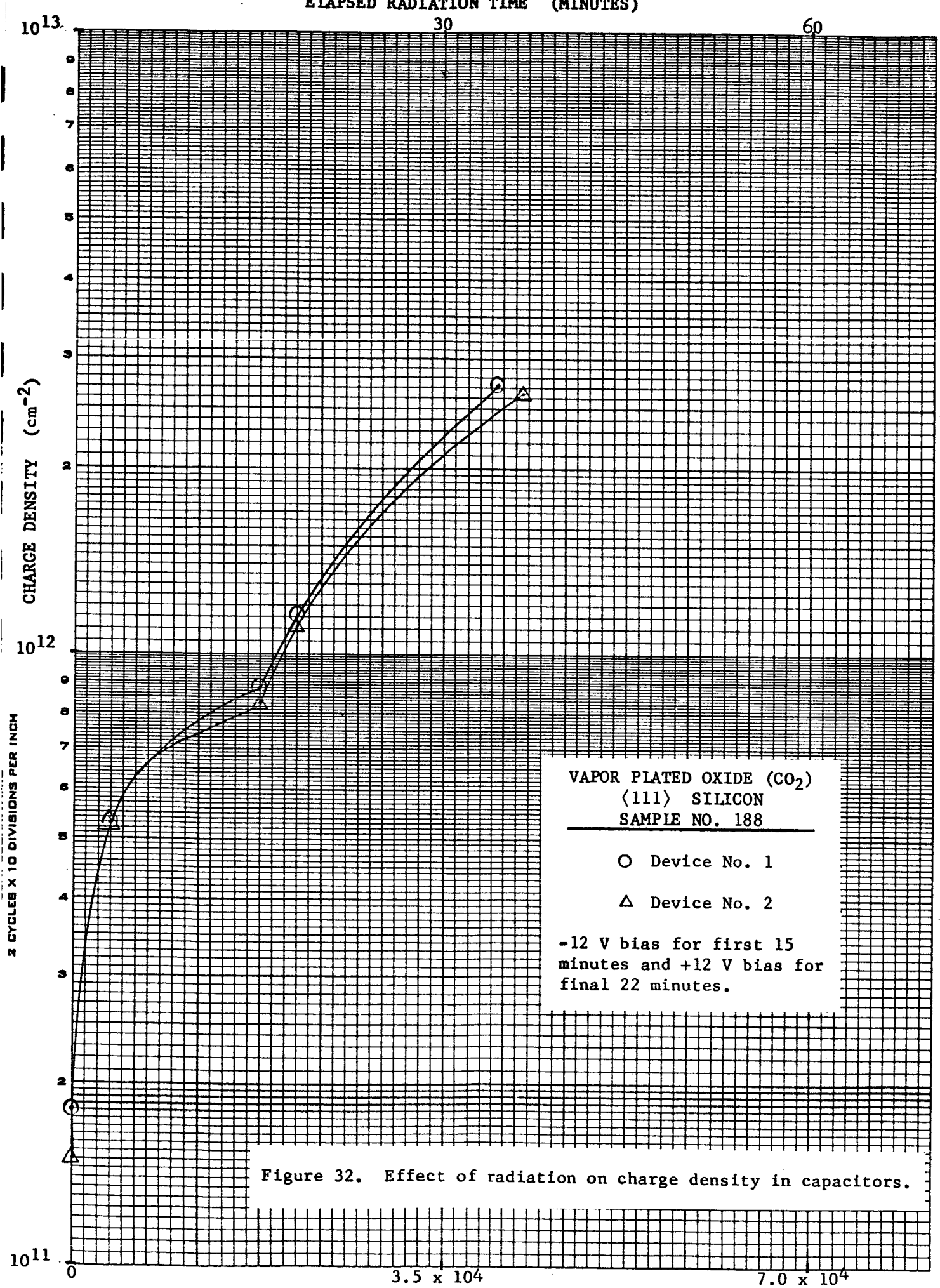


Figure 32. Effect of radiation on charge density in capacitors.

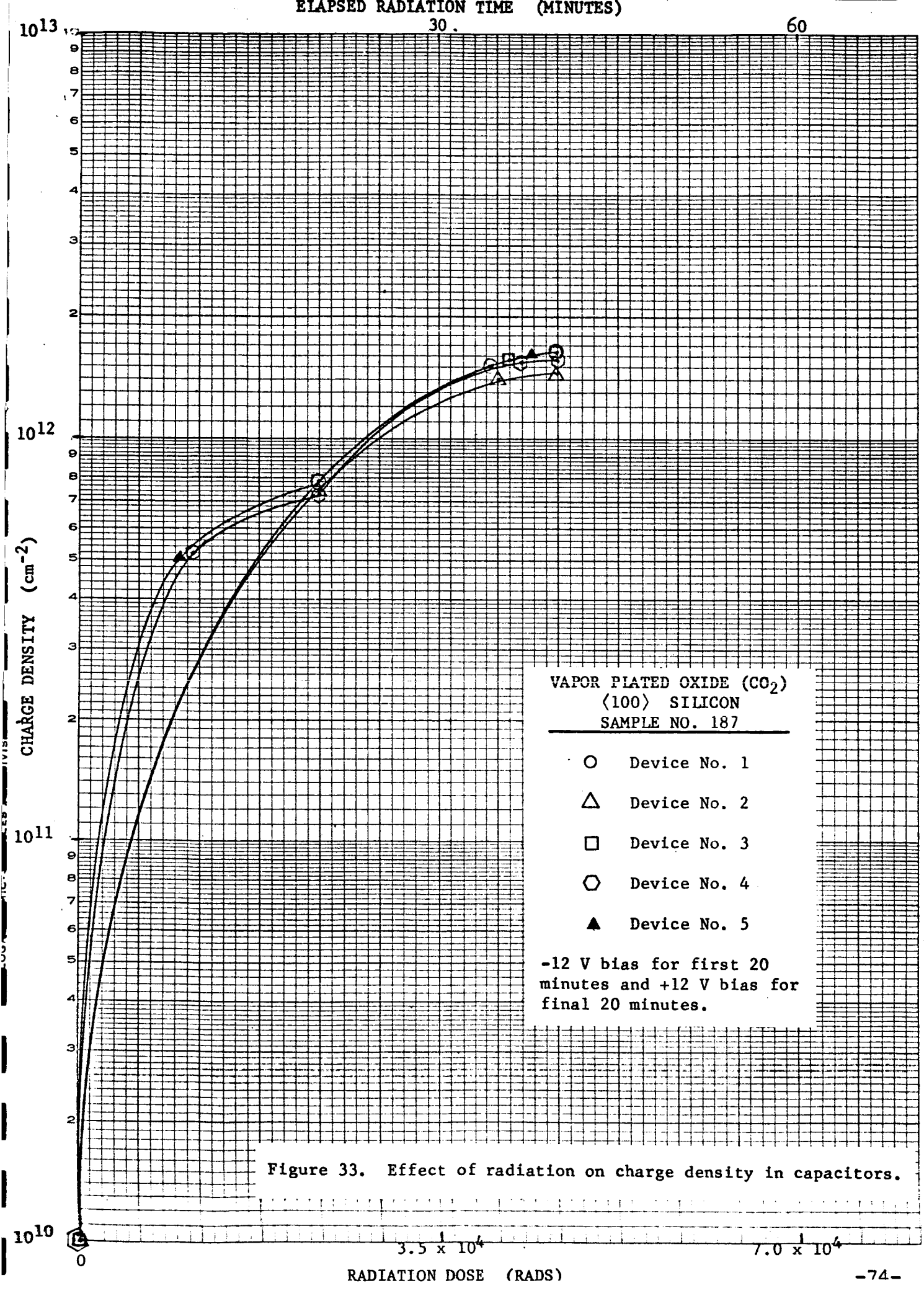


Figure 33. Effect of radiation on charge density in capacitors.

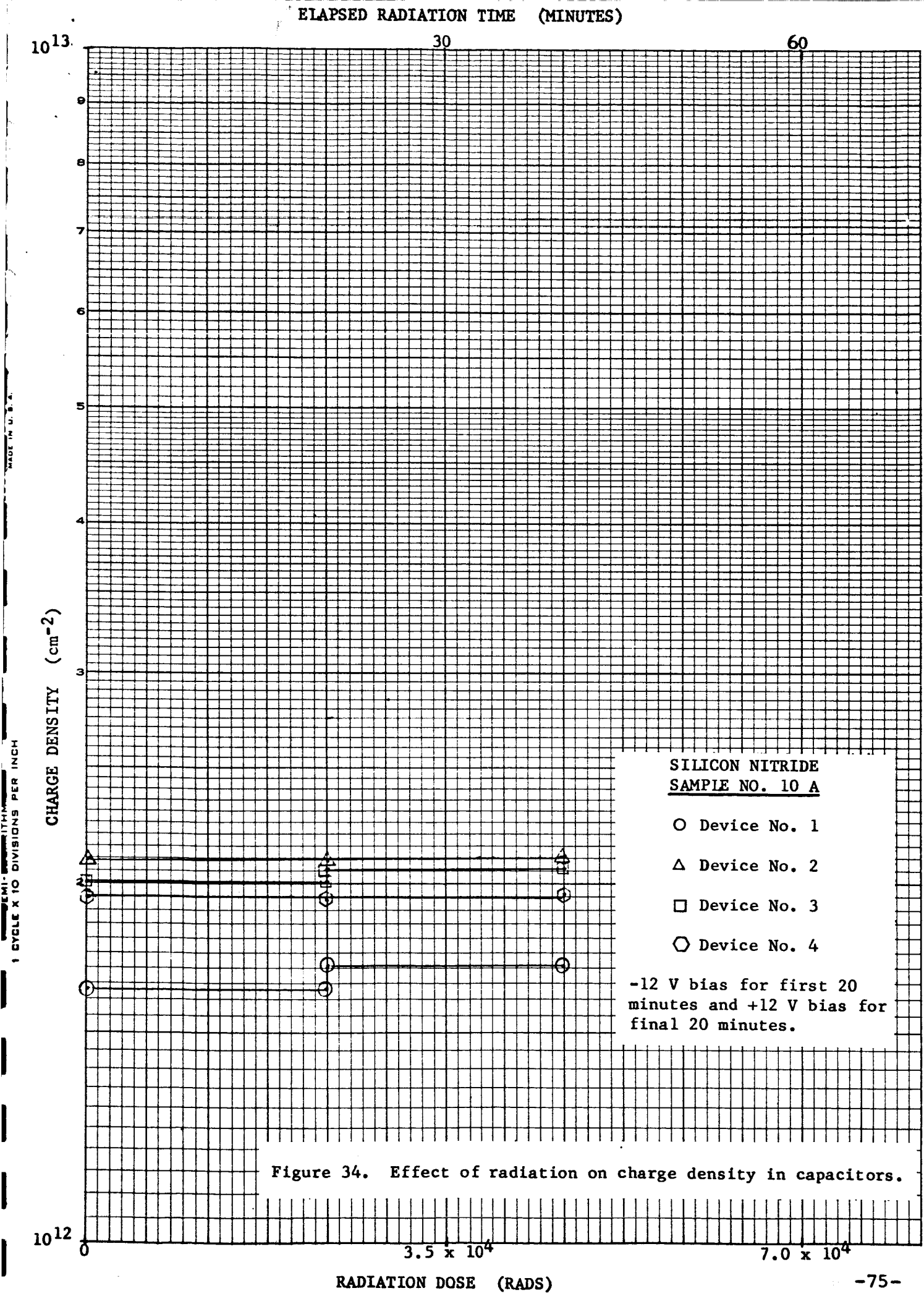


Figure 34. Effect of radiation on charge density in capacitors.

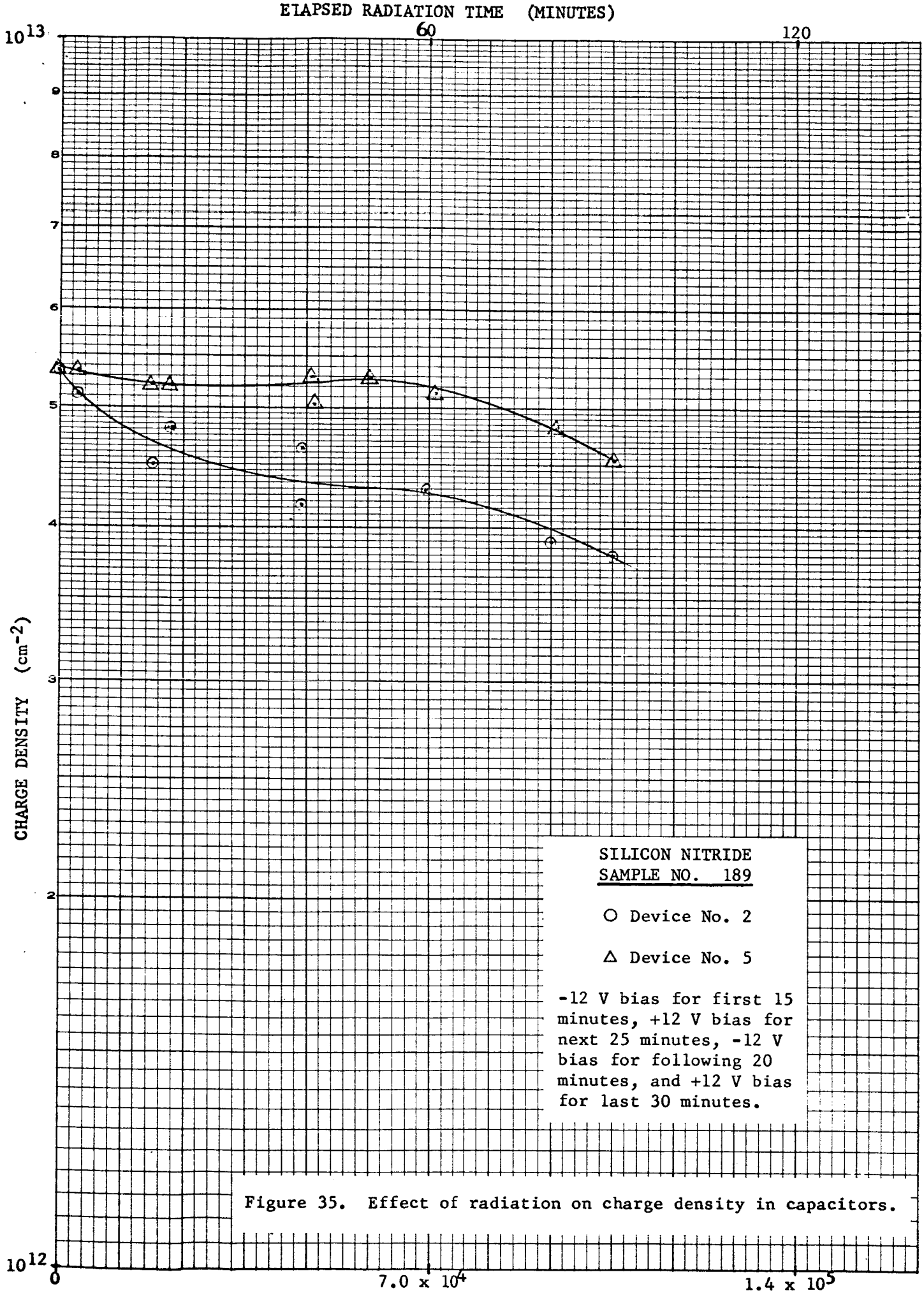


Figure 35. Effect of radiation on charge density in capacitors.

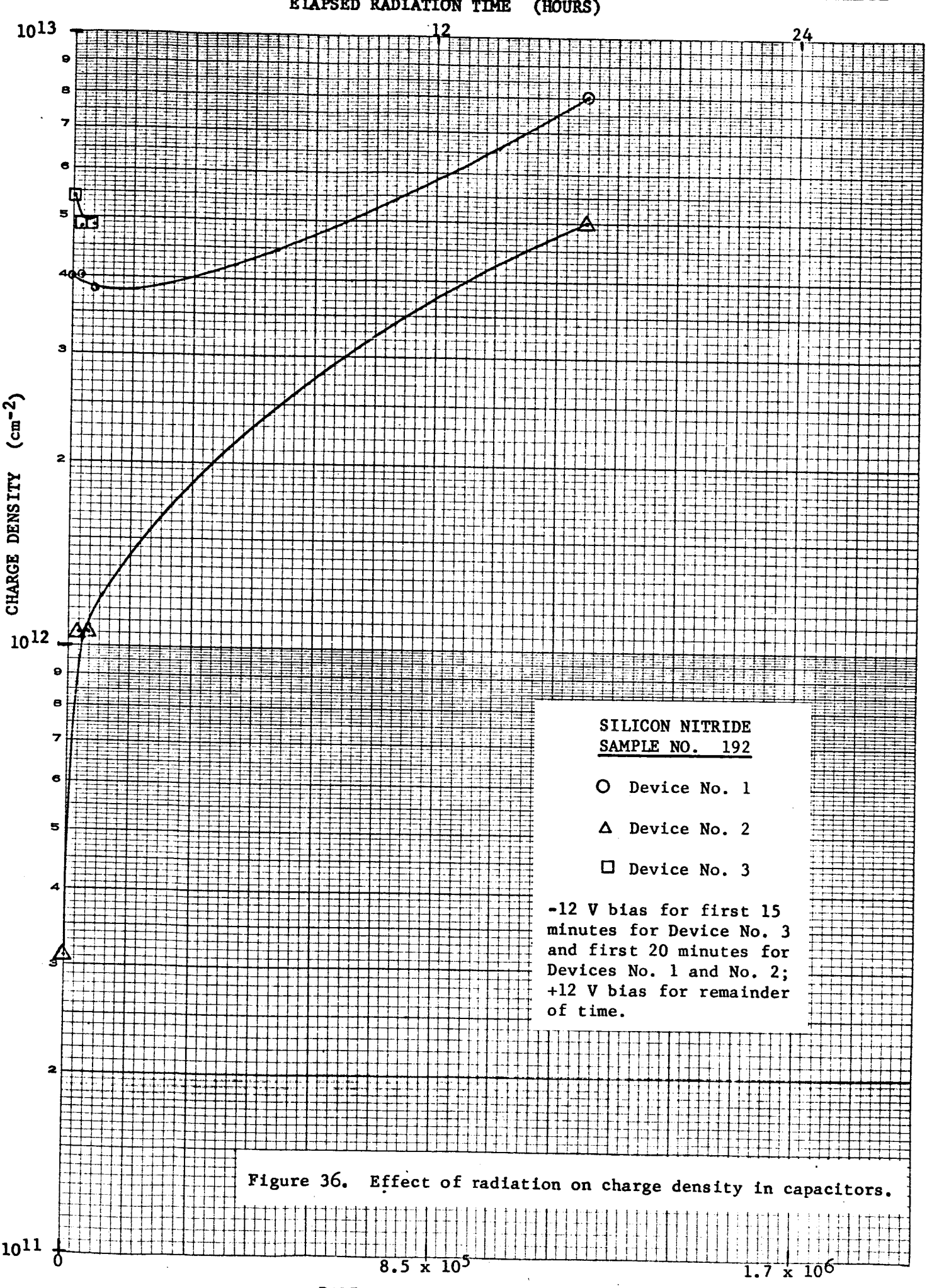


Figure 36. Effect of radiation on charge density in capacitors.

reported that low energy electron irradiation induces much less charge in the insulating layer of capacitors made with silicon nitride than in those made with silicon oxide. They find that the irradiation affects the charge density in the insulator layer in a way that can be interpreted to be due to the trapping of electrons.

Figures 37 to 44 show the effects of gamma radiation on the threshold voltage and on the transconductance of p-channel MOS transistors.

These figures show the following:

1. The radiation induced degradation in threshold voltage and in transconductance is very similar for thermally grown oxides and for vapor plated oxides.

2. The radiation induced degradation in threshold voltage and in transconductance is independent of the silicon orientation.

3. Several Fairchild (FI100) p-channel MOS transistors showed a decrease in threshold voltage during irradiation under a negative 12 V bias. There was a significant amount of degradation in threshold voltage during an irradiation under positive bias.

4. p-channel MOS transistors, fabricated with a process involving a phosphorus deposition followed by heat treatment and subsequent removal of most of the phosphorus containing oxide, have exhibited a significantly higher resistance to radiation (both for threshold voltage and for the transconductance).
These transistors were fabricated on a related company sponsored program. Introduction of the phosphorus into these oxides was accomplished as follows. The oxide was grown to a thickness of about 5000 Å at 1200° C in a sequence of dry O_2 for 25 minutes, wet O_2 for 30 minutes, and dry O_2 for 15 minutes. The oxide was removed from the back of the wafer which was afterward electroless nickel plated. Then a phosphorus deposition was made at 1080° C for 17 minutes from a $POCl_3$ source. The sample was heated at 1080° C for 6 minutes in wet O_2. It was next heated to 1200° C for 20 minutes in dry O_2 followed by 20 minutes in dry N_2. The oxide was then etched back to 1300 Å in the gate region.
Considering the processing schedule, the amount of phosphorus remaining in the oxide must have been small.

The effect of the phosphorus may have been to getter impurities from the oxide.

The leakage current of the drain to substrate junction was not affected by the irradiation dosages involved in this work.

We irradiated some p-channel MOS transistors and some MOS capacitors on n-type silicon at -78° C and at +95° C. We found no temperature dependence in the degradation of the threshold voltage of the transistors or in the shift of the C-V curve for the capacitors.

Figure 45 shows a measure of the rate at which transistors can be annealed after an irradiation.

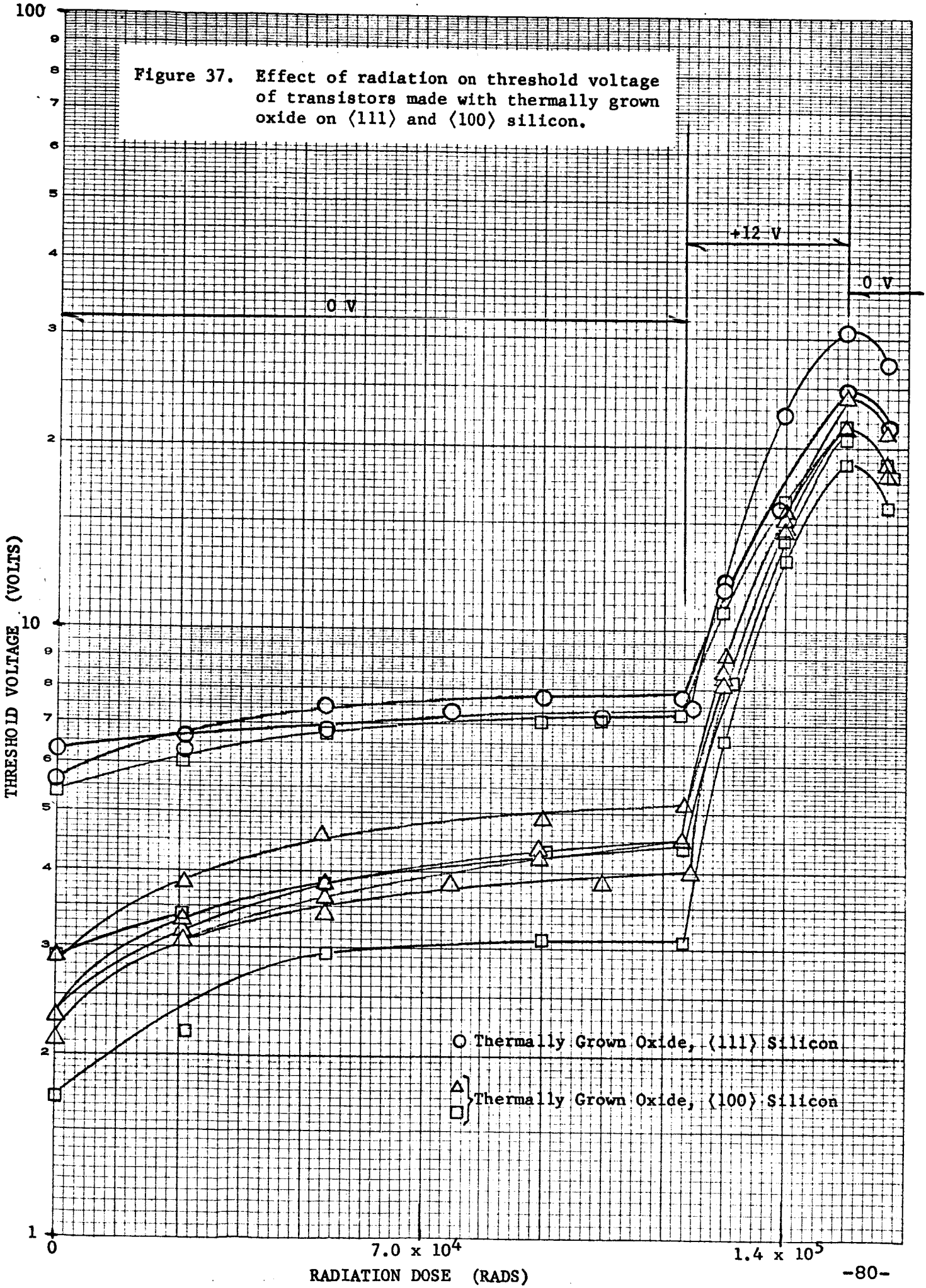


Figure 37. Effect of radiation on threshold voltage of transistors made with thermally grown oxide on ⟨111⟩ and ⟨100⟩ silicon.

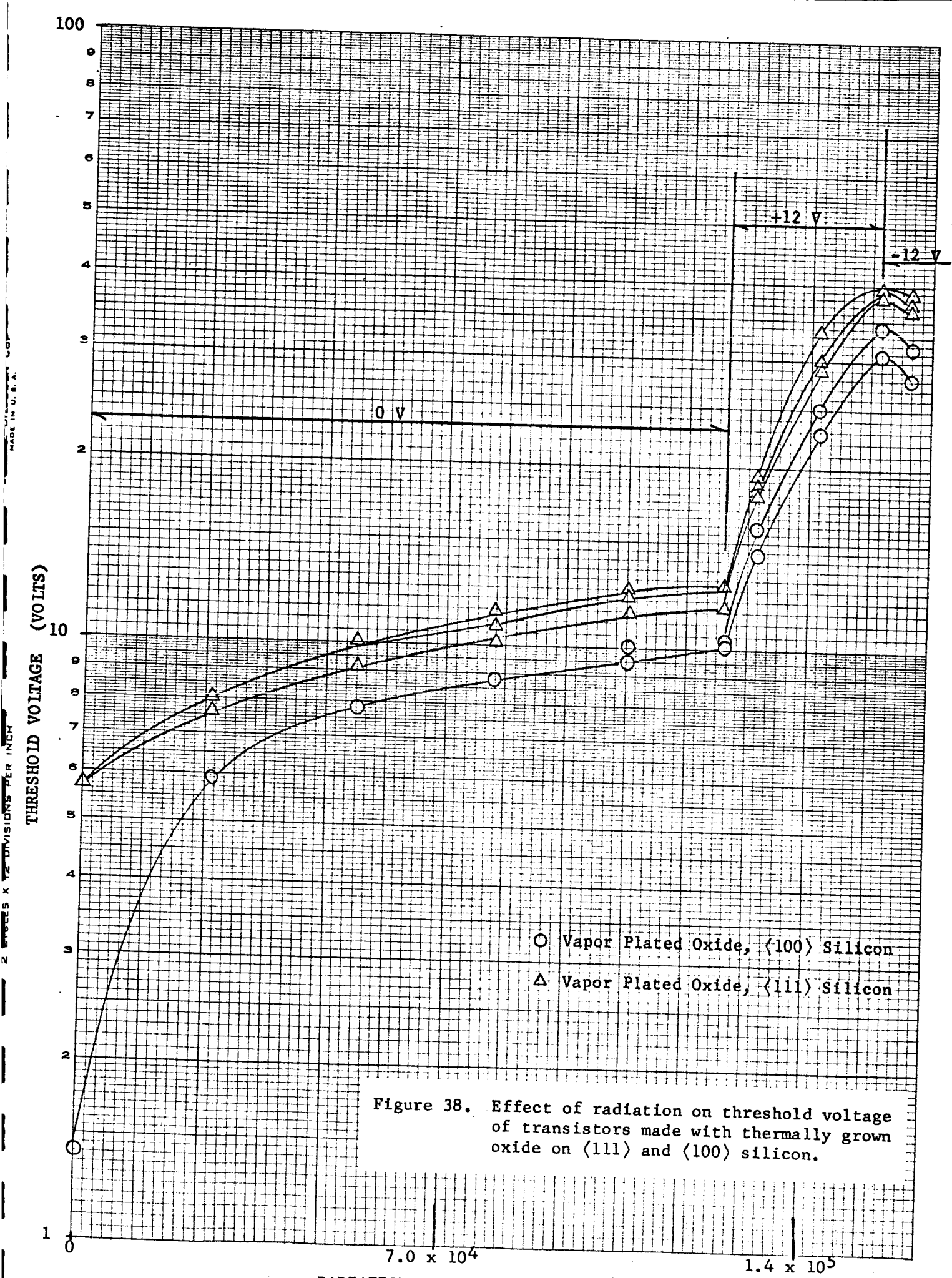


Figure 38. Effect of radiation on threshold voltage of transistors made with thermally grown oxide on ⟨111⟩ and ⟨100⟩ silicon.

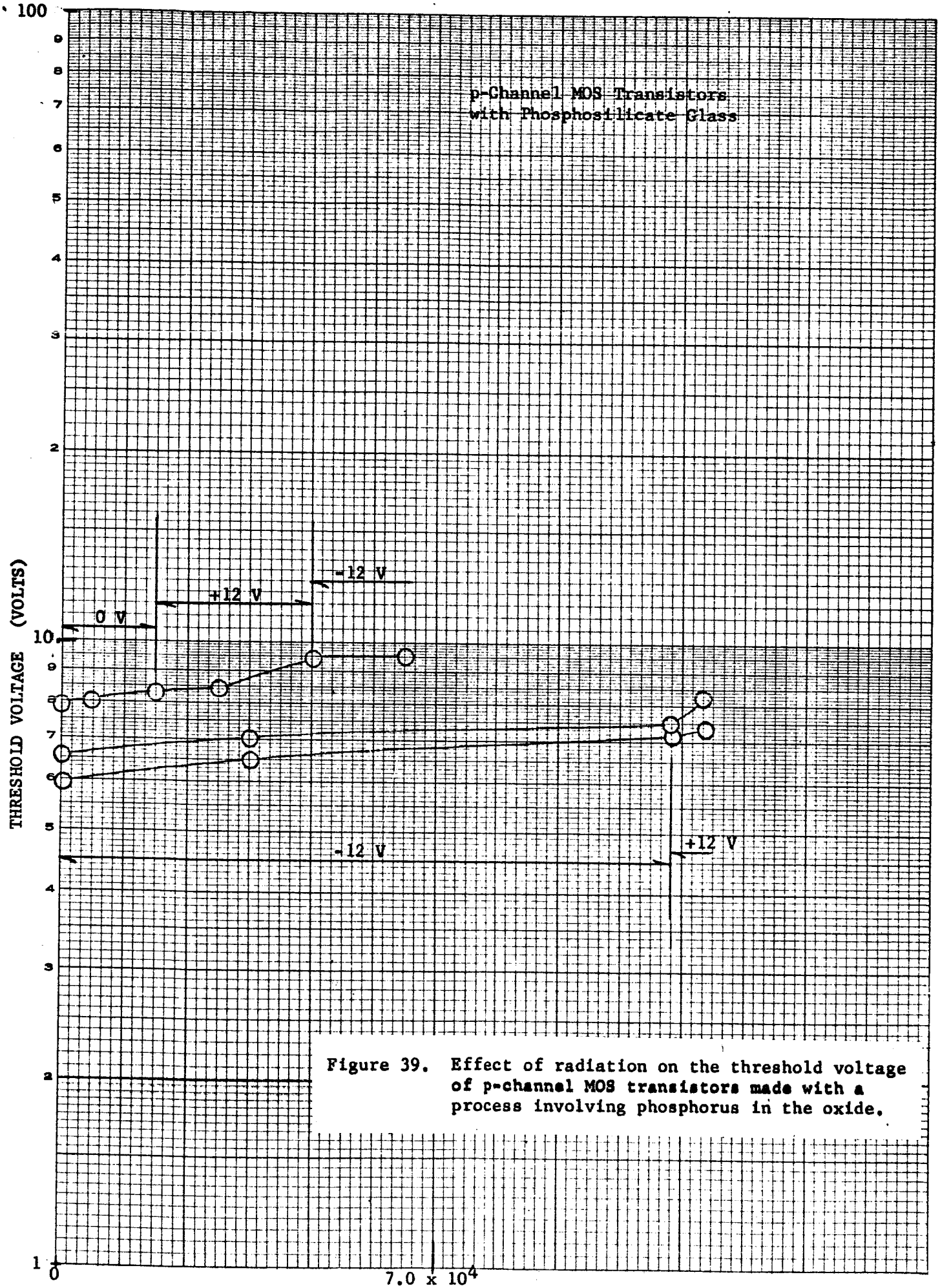


Figure 39. Effect of radiation on the threshold voltage of p-channel MOS transistors made with a process involving phosphorus in the oxide.

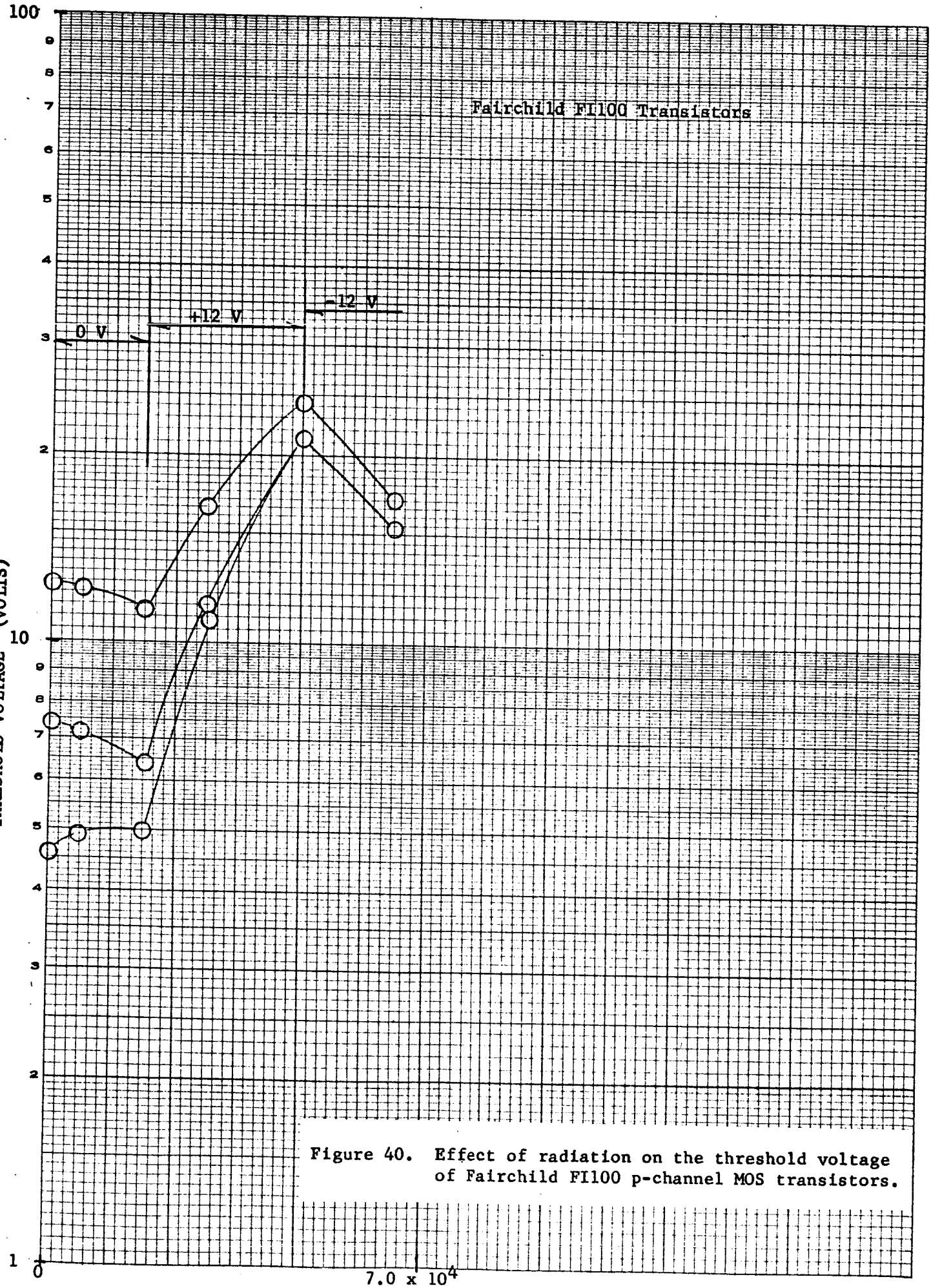


Figure 40. Effect of radiation on the threshold voltage of Fairchild FI100 p-channel MOS transistors.

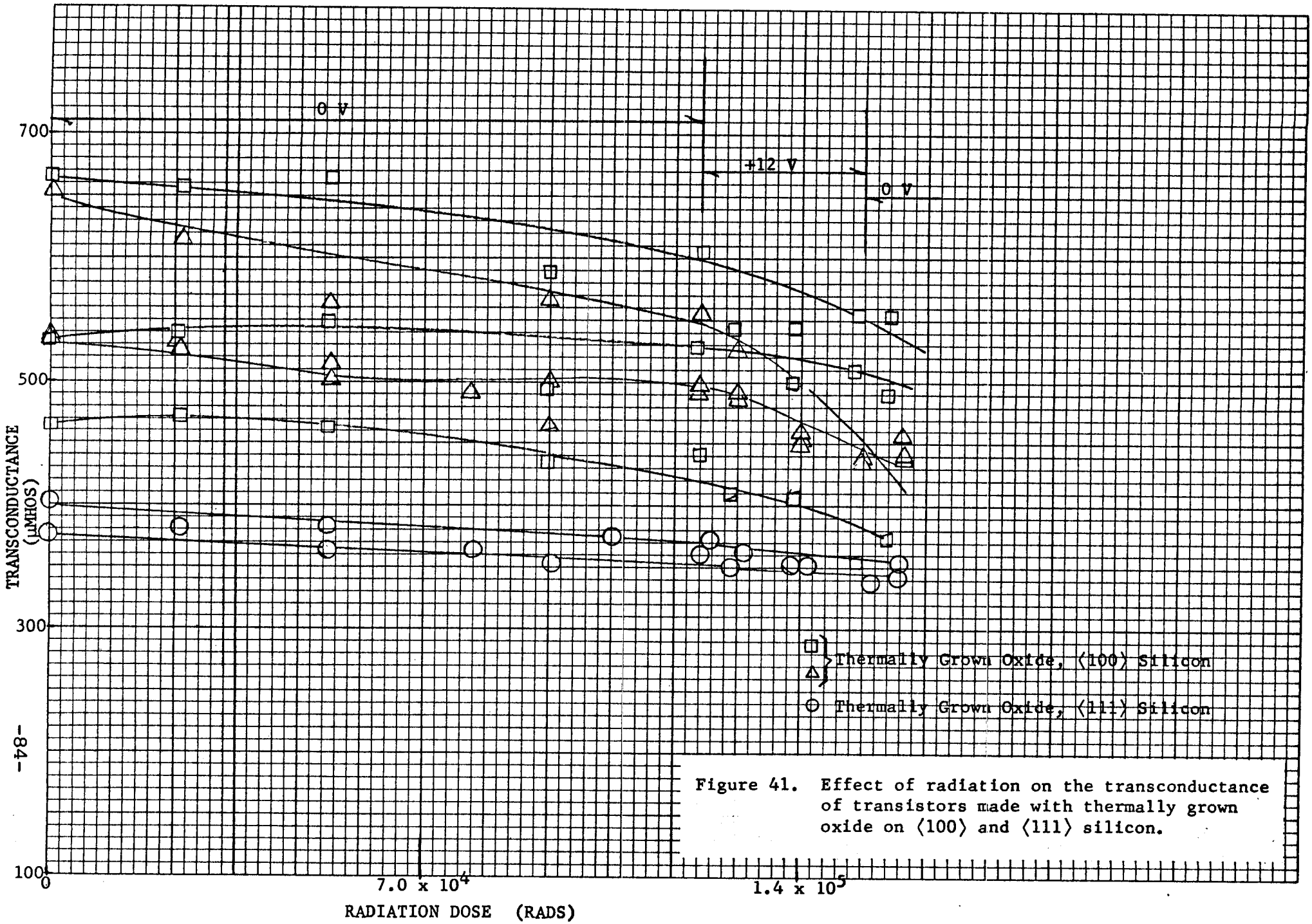


Figure 41. Effect of radiation on the transconductance of transistors made with thermally grown oxide on ⟨100⟩ and ⟨111⟩ silicon.

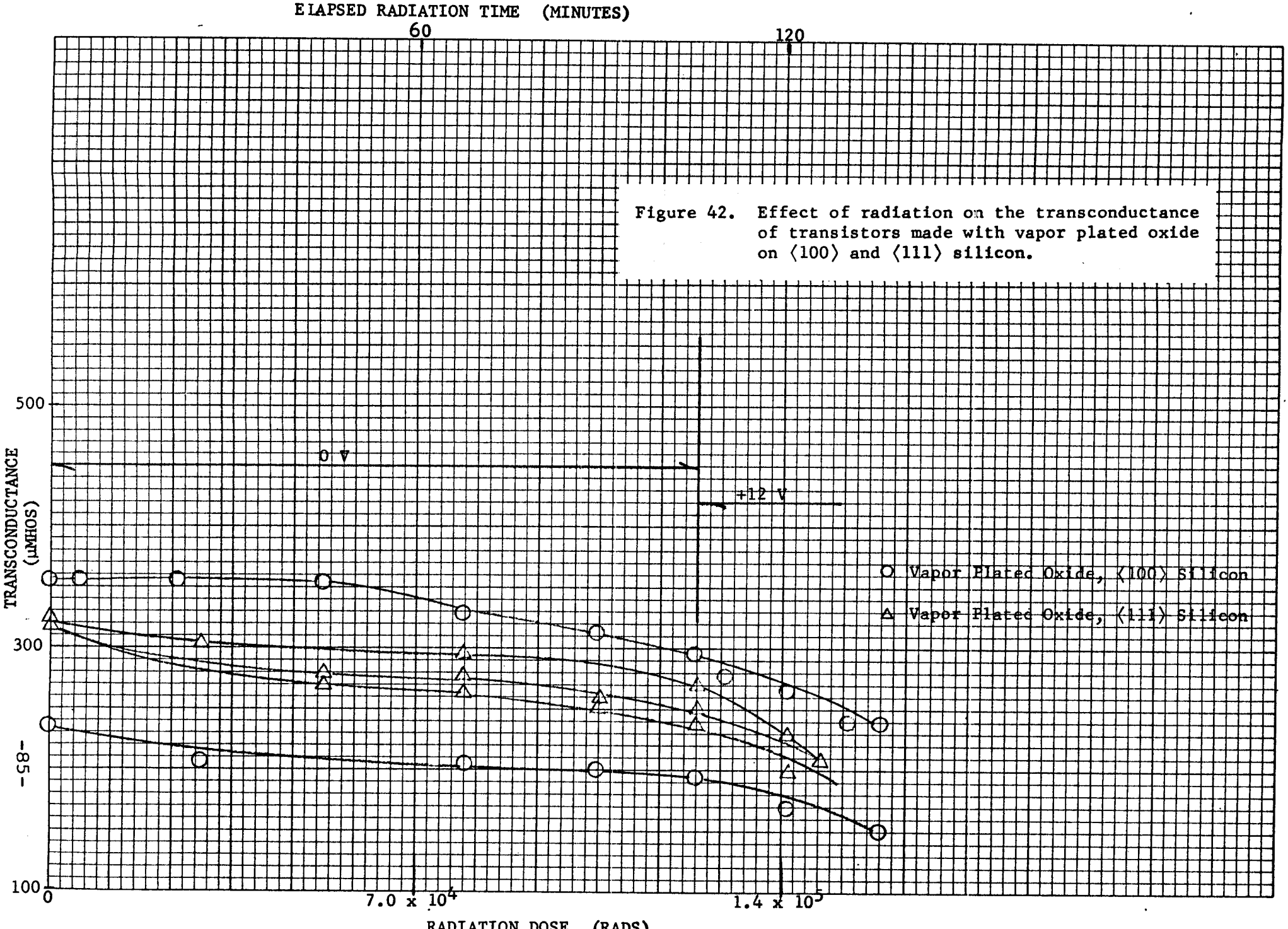


Figure 42. Effect of radiation on the transconductance of transistors made with vapor plated oxide on ⟨100⟩ and ⟨111⟩ silicon.

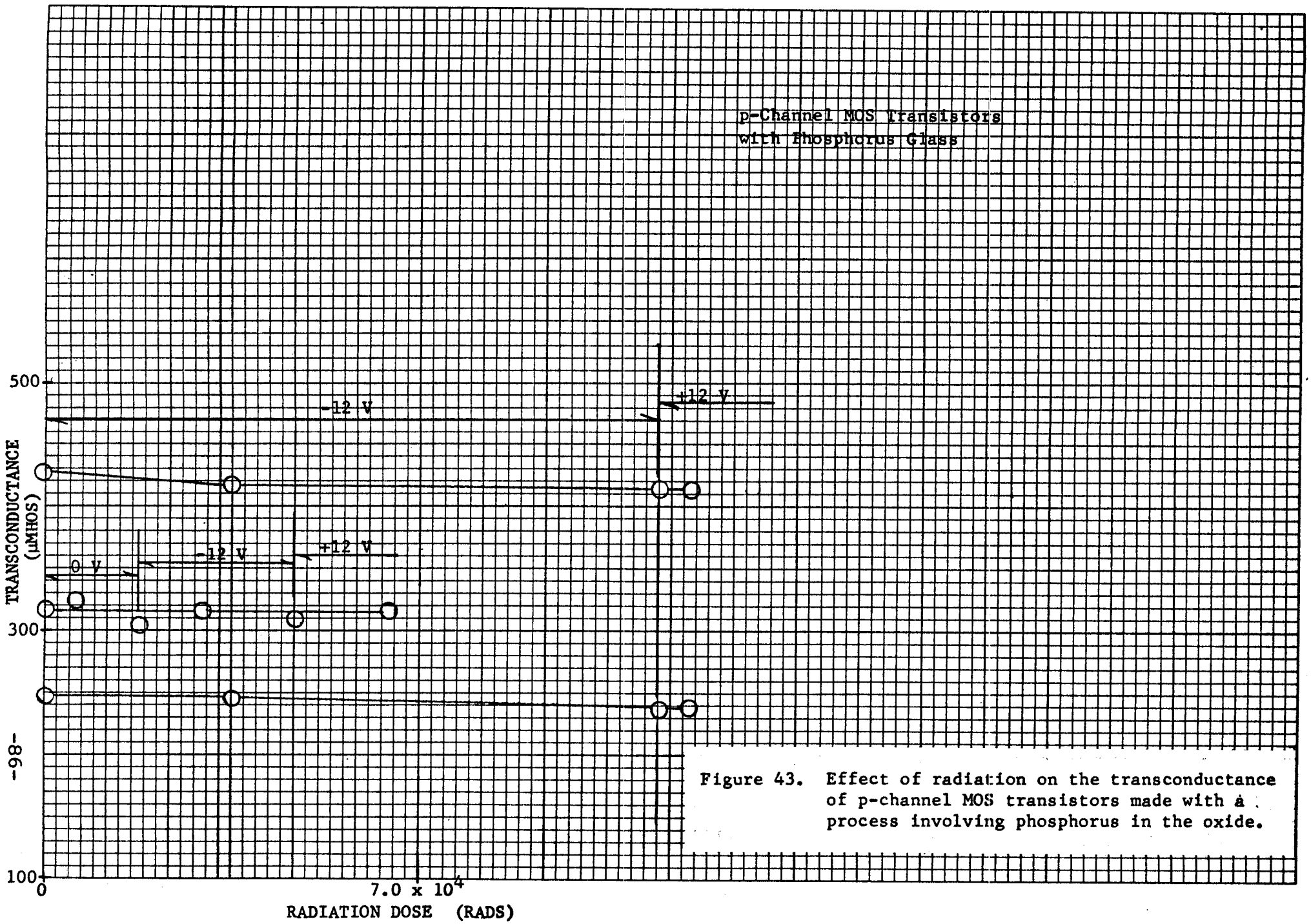


Figure 43. Effect of radiation on the transconductance of p-channel MOS transistors made with a process involving phosphorus in the oxide.

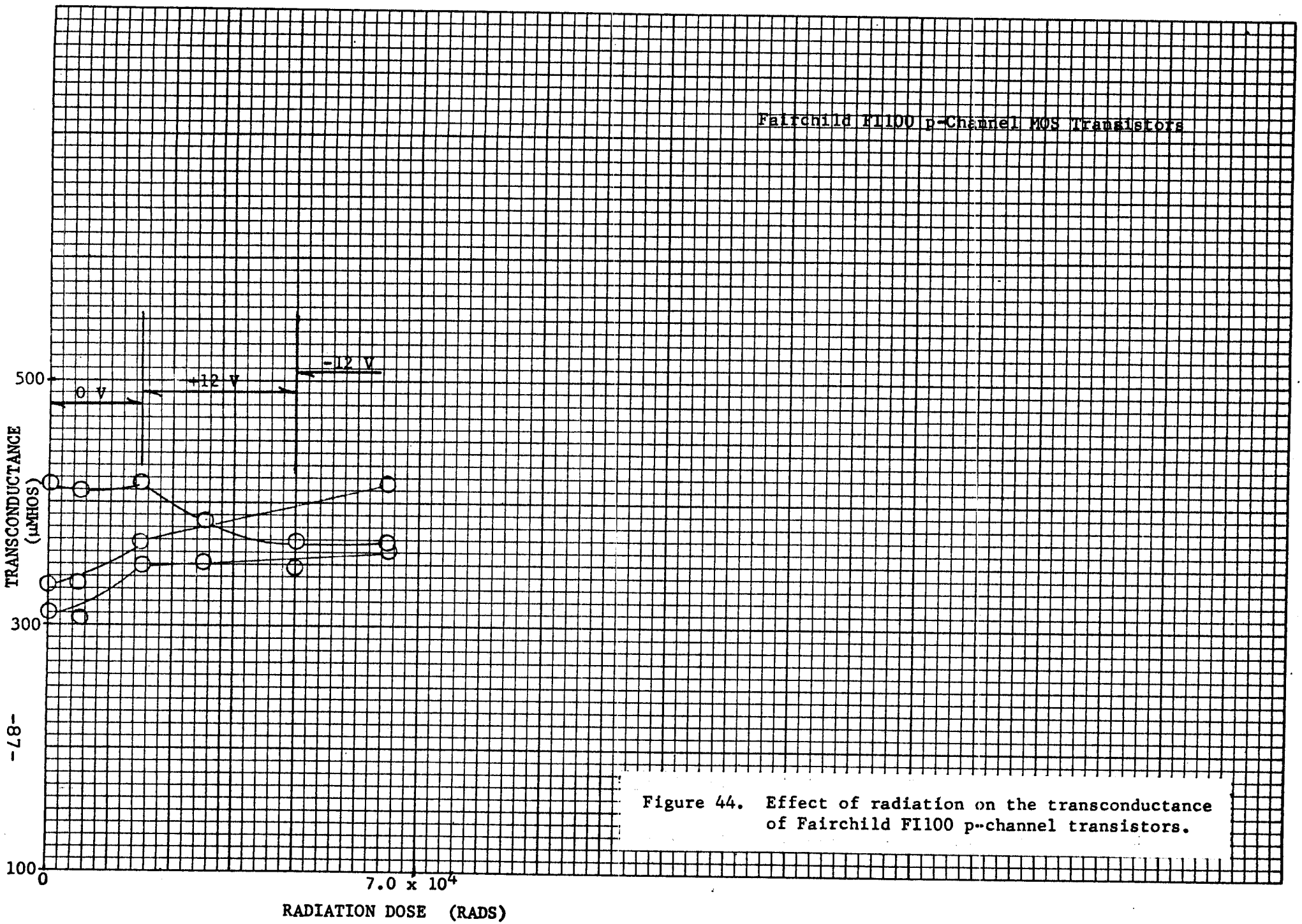


Figure 44. Effect of radiation on the transconductance of Fairchild FI100 p-channel transistors.

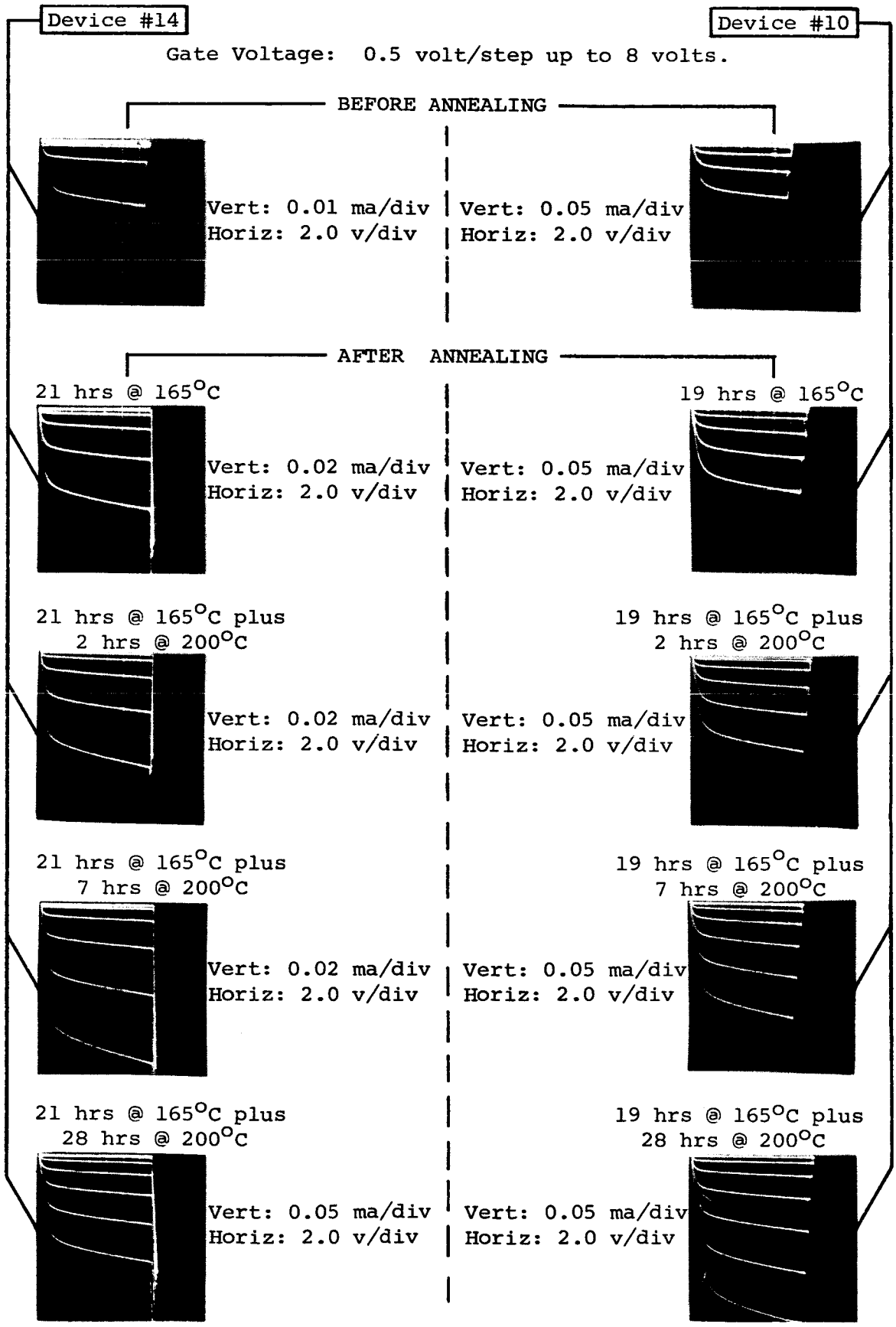


Figure 45. Annealing of MOS transistors after gamma irradiation.

6. EFFECTS OF WATER ON OXIDE PROPERTIES

6.1 Introduction

Water has been shown to affect MOS device stability, threshold voltage, radiation sensitivity[114] and the density of trapping states[114]. It is likely that water has been responsible for many of the differences found in the experimental results reported by various investigators. This section describes several experimental efforts that were made during the program to establish more clearly the conditions in which water is absorbed in oxides.

The equipment described in subsection 2.1 enabled us to prepare thermal oxides with a substantially reduced water content. Such dry oxides were exposed to room air under various conditions to determine those in which water significantly affects the oxide properties.

6.2 Diffusion of Water Into the Oxide

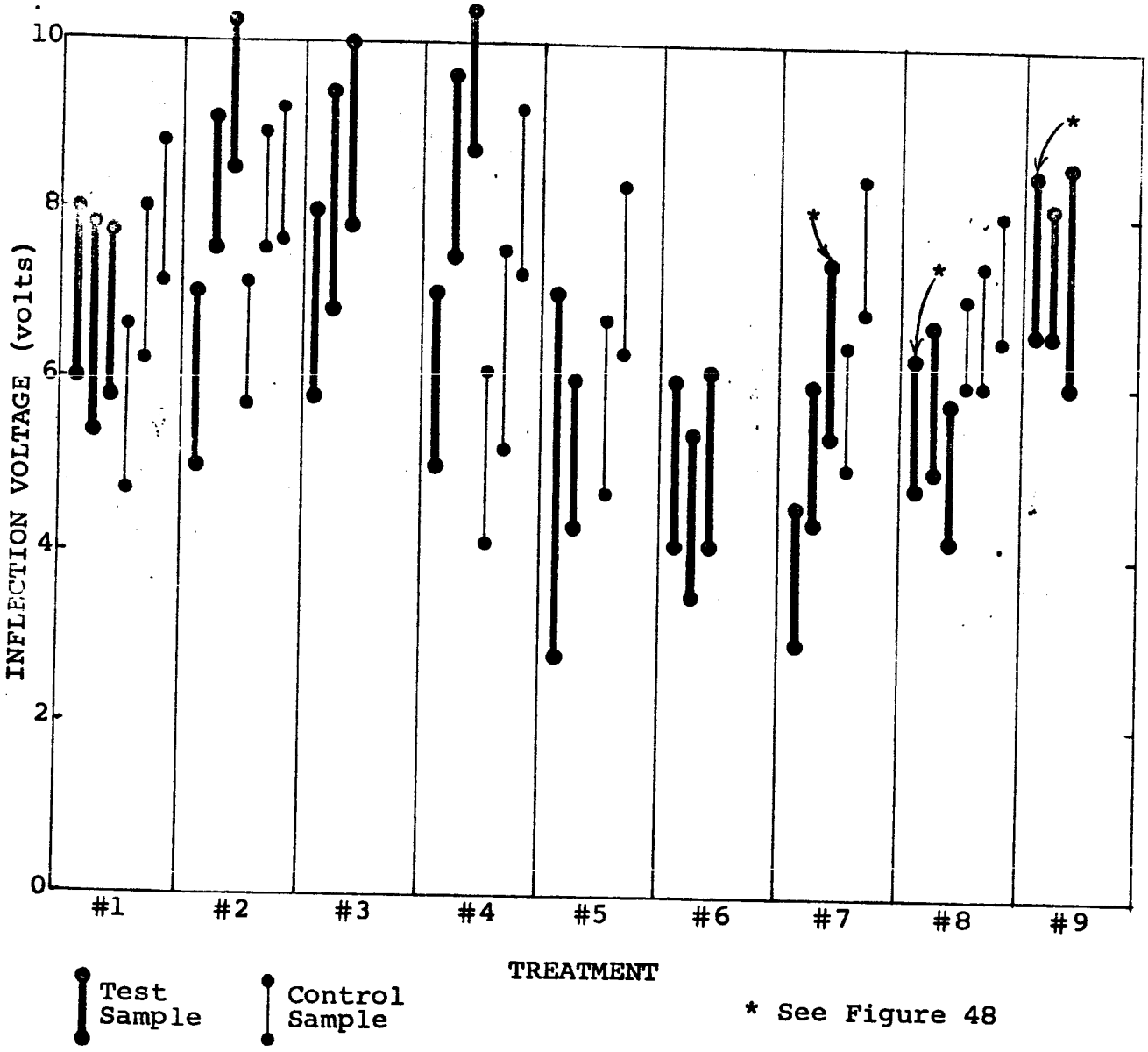
In one experiment an oxide was grown thermally to a thickness of 2000 Å on each of two halves of a 5 Ω-cm phosphorus doped silicon wafer. One-half was the test sample, which was subjected to a sequence of exposures to room air, while the other half served as the control. Measurements were taken in the form of capacitance-voltage curves measured at a frequency of 140 kHz with a gold ball probe, after each of the following drifting steps:

1. -30 V, 1 min., 22°C, and

2. +30 V, 1 min., 22°C.

The drift saturated in time intervals shorter than 1 minute and the observed shifts of the C-V curves were reproducible. Figure 46 summarizes the experimental results. The variation in the inflection voltage (first an increase and later a decrease) of the test sample has not been explained. This data indicates that minute amounts of water did not significantly affect the immobile or the mobile charge density.

On the other hand, a change was observed in the state density in the oxide. This state density can be qualitatively evaluated by an examination of the steepness of the slope of the C-V curve in the transition region. The explanation for this is:



DESCRIPTION OF TREATMENT OF TEST AND CONTROL SAMPLES

Test Sample:

#1 Initial measurements.
#2 After 10 min. in room air.
#3 After 16 hr. in dry box.
#4 After 1 hr. in room air.
#5 After 19 hr. in room air.
#6 After 7 days in dry box.
#7 After 18 hr. in room air and a subsequent bake at 300° C for 1 hr. in the dry box.
#8 After a bake at 400° C for 1 hr. in dry N_2.
#9 After a bake at 400° C for 1 hr. in room air.

Control Sample: The control sample was kept in the dry N_2 at room temperature and tested after most of the treatments in the test sample sequence. The control sample was given the same temperature treatments as the test sample, i.e., 300° C for 1 hr. in treatment #7, and 400° C for 1 hr. in treatment #8.

Figure 46. Summary of C-V data from experiment to determine the effects of exposure to room air.

Trapping states are assumed to exist in the oxide or at the oxide-silicon interface. The state of occupancy of each of these traps depends on the electrostatic potential at each of the trap sites. This potential in turn depends on the applied voltage. As the applied voltage is varied, the occupancy of the traps changes. This changes the density of charge in the oxide. If the charge density of the oxide changes during the recording of the C-V curve, the C-V curve will have a gradual slope in the transition region.

Figure 47 shows C-V curves taken on two oxides with different levels of water content. These curves were taken on unmetalized oxides with a gold probe. Sample #115 was cooled in the modified oxidation tube designed to minimize the moisture content, whereas #116 was cooled at the end of the tube in the regular way. Sample #115 is therefore a drier oxide. These curves illustrate that drier oxides have higher trapping state densities. On this basis, one can examine the shapes of the C-V curves taken in the experiment conducted to determine the effect of room air on oxides (i.e., the curves from which Figure 46 was prepared). Figure 48 presents tracings of C-V curves taken at the beginning of the experiment, and just before and just after the bakes at 300°C for 1 hour in dry nitrogen and at 400°C for 1 hour in room air. These tracings clearly show that the curve shapes did not change significantly during the sequence of treatments until the bakes at 300°C and 400°C. This indicates that moisture does not diffuse into the oxide at room temperature in room air for a period of time up to 40 hours, and that moisture does diffuse into the oxide at 400°C in room air. This agrees with the observation of Kooi[114] that treatments in wet ambients at 450°C decrease the number of surface states.

The observations described above indicate that the diffusion of water in oxides on silicon is similar to that reported by Moulson and Roberts[157] for water in silica glass. They studied the diffusion coefficient for the entry of infrared absorbing centers in silica glass heated in water vapor between 600 and 1200°C. They found that this diffusion coefficient obeys the equation

$$D = 1.0 \times 10^{-6} \exp(-18300/RT) \text{ cm}^2/\text{sec.}$$

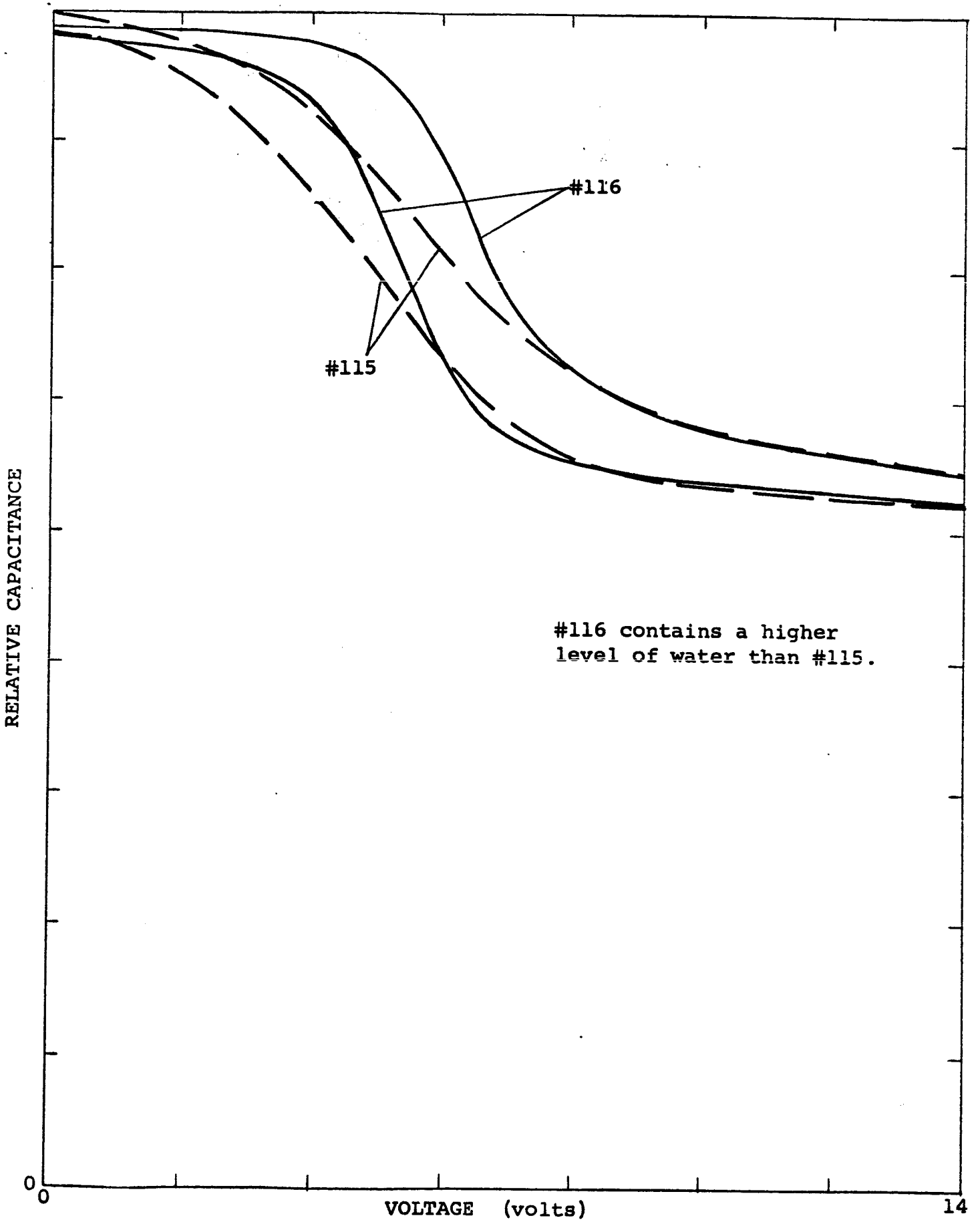
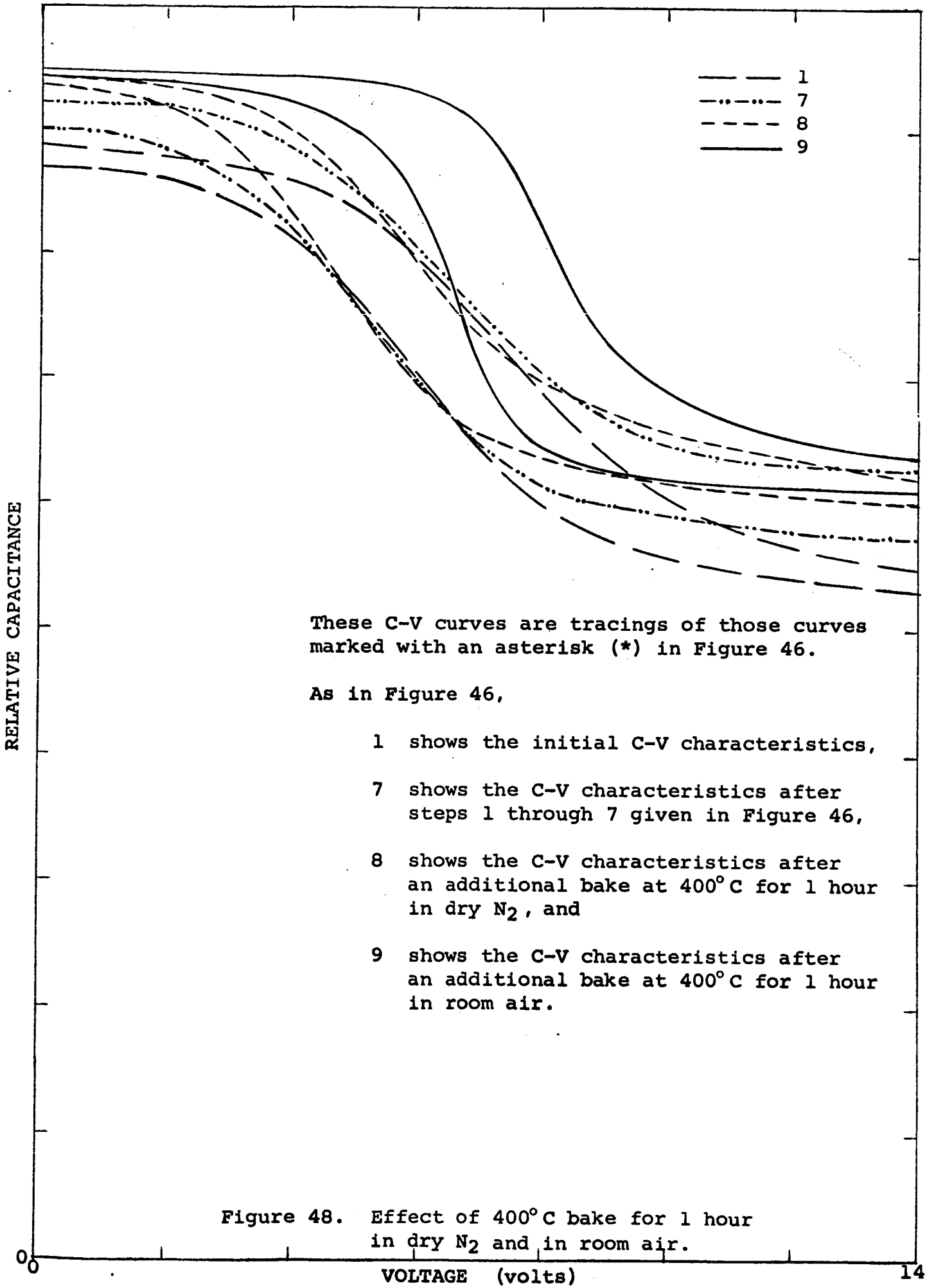


Figure 47. C-V curves taken on two oxides with different levels of water content.



These C-V curves are tracings of those curves marked with an asterisk (*) in Figure 46.

As in Figure 46,

1 shows the initial C-V characteristics,

7 shows the C-V characteristics after steps 1 through 7 given in Figure 46,

8 shows the C-V characteristics after an additional bake at 400°C for 1 hour in dry N_2, and

9 shows the C-V characteristics after an additional bake at 400°C for 1 hour in room air.

Figure 48. Effect of 400°C bake for 1 hour in dry N_2 and in room air.

If we assume this equation to hold at lower temperatures and that the diffusing species is the same as that with which we are concerned, we can calculate diffusion coefficients to be

$$D_{27°C} = 5.1 \times 10^{-20} \text{ cm}^2/\text{sec.},$$

$$D_{300°C} = 1.2 \times 10^{-13} \text{ cm}^2/\text{sec., and}$$

$$D_{400°C} = 1.1 \times 10^{-12} \text{ cm}^2/\text{sec.}$$

The diffusion lengths calculated from the equation

$$L = \sqrt{Dt},$$

for a diffusion time of 24 hours are

$$L_{27°C} = 6.6 \text{ Å},$$

$$L_{300°C} = 10100 \text{ Å, and}$$

$$L_{400°C} = 30800 \text{ Å}.$$

Clearly, these values are consistent with our experimental observations that although diffusion does not seem to be important at room temperature, it is important at 400°C.

6.3 Increase in Immobile Charge Density Due to Heat Treatments in Wet Ambients

It was shown that the presence of water at high temperatures, i.e., greater than 400°C, can cause a large increase in immobile charge density. This was first observed as part of a series of experiments designed to determine the effects of high temperature baking and of variations in the post-bake cooling rate. Data taken in this effort is given in Tables 7, 8, and 9. The voltages are the voltages at the point of inflection of the C-V curve. The results of other experiments show that the increases in charge density indicated in Tables 7, 8, and 9 depend on the absorption of water from room air that had back-flowed into the oxidation furnace at the end in which the oxides were being cooled.

TABLE 7

EFFECTS OF POST-OXIDATION BAKE AND COOLING RATE (n-Type Si)

Step	Treatment	Transition Voltage (volts)
1.	3000 Å oxide, bake 24 hours in N_2 at 1200° C, fast removal from furnace.	12 - 17
2.	Return to furnace and remove slowly over a 1-hour period.	31 - 32
3.	Return to furnace, fast removal from furnace; repeat three times.	6.4-7.8
4.	Return to furnace, slow removal over a 2-hour period.	8.0-10.6
5.	Return to furnace, bake 15 hours in N_2 at 1200° C; slow removal over a 2-hour period.	35 - 40
6.	Return to furnace, bake 15 minutes in O_2 at 1200° C; fast removal from furnace.	6.4-7.2

TABLE 8

EFFECTS OF POST-OXIDATION BAKE AND COOLING RATE (p-Type Si)

	Step	Treatment	Transition Voltage (volts)
Sample #1	1.	Regular Planar II oxide, 3000 Å, fast removal from furnace.	6 - 8
	2.	Return to furnace, remove slowly over 1-1/2-hour period.	8.2-9.4
Sample #2	1.	Regular Planar II oxide, 3000 Å, 24 hours in N_2 at 1200° C, remove slowly over a 1-hour period.	36 - 45
	2.	Return to furnace, remove quickly; repeat three times.	22.4-32.8
	3.	Return to furnace, remove slowly over 1-1/2-hour period.	23.2-28.8

TABLE 9

EFFECTS OF POST-OXIDATION BAKE IN N_2 AND He (n-Type Si)

Step	Treatment	Transition Voltage (volts)
1.	Initial.	6.0 - 6.8
2.	After 2 hours in tank helium at 1200° C.	11.6 - 11.7
3.	After 2 hours in nitrogen at 1200° C.	34 - 39
4.	After 16-1/2 hours in tank helium at 1200° C.	8.4 - 8.8
5.	After 1 hour in dry helium* at 1200° C.	11.8 - 15.4
6.	After 4 hours in dry helium at 1200° C.	8.8 - 9.0

* Dry helium is tank helium run through a liquid nitrogen-cooled cold trap filled with Molecular Sieve.

Two oxide samples (#117 and #118) were prepared by thermal oxidation in dry O_2 at 1200°C followed by a 16 hour bake in dry N_2 at 1200°C after which they were removed from the furnace through the gas inlet end of the tube so they were very dry. The oxides were evaluated in the unmetalized state with the gold ball probe. Sample #117 had an initial inflection voltage of 4 to 5 V, a value which is fairly typical for 2000 Å thick thermally grown oxides on <111> silicon. This sample was baked at 1200°C in dry O_2 for 15 minutes and then removed through the gas outlet end of the tube where room air moisture was present. After this treatment the inflection voltage was 16 to 17 V. The bake for 15 minutes in dry O_2 at 1200°C was repeated but this time the sample was removed slowly over a 1-hour period. The inflection voltage was 17 to 18 V. The sample was again put into the 1200°C, dry O_2 for 15 minutes and then removed through the gas inlet end of the tube. This reduced the inflection voltage to about 8 to 9 V indicating that some of the water could still be removed in a 1200°C bake in dry O_2.

Another oxide (#118) was similarly prepared except that after the 16-hour bake in N_2 it was slowly cooled over a 1-hour period in the gas inlet (dry) end of the tube. This oxide sample exhibited initial inflection voltages of 2 to 4 V. After a 15-minute bake at 1200°C in dry O_2, and a slow cool (1-1/2 hours) through the gas outlet end of the tube, the inflection voltage was 8 to 14 V. This oxide was subsequently baked at 1200°C for 10 minutes in dry O_2 and slowly cooled in the gas inlet end of the tube. In this case, the inflection voltage increased to 16 to 17 V.

These results show that the immobile charge density in an oxide can be increased by a bake at high temperatures in the presence of water. Apparently this is reversible in some cases but not in all cases.

6.4 Effect of Heat Treatment at 300°C on Immobile Charge Density is Independent of Water Content

In Figure 23 we show that the immobile charge density is decreased by baking the oxidized silicon at 300°C for one hour. This decrease in immobile charge density occurs in very dry oxides that are baked in dry N_2 for one hour, showing that this effect is not related to the presence of water.

6.5 Experiment with Tritiated Water

As the importance of water became more apparent, consideration was given to the possibility of using tritiated water for exploring in detail the effects of water on the properties of oxides. Dr. S.S. Choi of the Philco Radiochemistry Laboratory calculated that tritiated water can be used to detect approximately 1.5×10^{13} water molecules per cm^2, either by counting or by autoradiographic techniques. An apparatus was constructed which permits the exposure of dry oxides to controlled pressure levels of tritiated water vapor at various oxide temperatures for long periods of time. The samples are heated by means of a radiant heater. The pressure of the tritiated water vapor was controlled by controlling the temperatures (below room temperature) of the liquid tritiated water.

Oxides were prepared to be very dry by means of the modified oxidation tube described in subsection 2.1. These oxides were then exposed to tritiated water vapor (10 curies/ml) at vapor pressures of approximately 10 mm of Hg at various temperatures from 300 to 600°C for time periods of the order of hours.

On some of these samples, with tritium-containing oxides on both sides, an aluminum metalization layer was evaporated on one side. The samples were heated in dry nitrogen at 400°C for 30 minutes, and then metal was removed by etching. The tritium count was then taken on each side of the sample as a function of the oxide thickness as the oxide was etched away in a sequence of etching steps. No difference was found in the profile of the tritium on the two sides of this sample. This indicates that any reaction involving aluminum, the oxide and the silicon does not significantly influence the distribution of the tritiated water in the oxide.

On other samples, both faces of the oxidized wafer were metalized. A voltage of 22.5 V was applied between the metal faces at a temperature of 350°C for 20 minutes. The sample was then cooled under bias. The metal was then etched away and the tritium distribution was profiled by counting between etching steps in which successive layers of oxide were removed. The profiles were found to be symmetrical on the two sides of the wafer, indicating that the applied field at the elevated temperature did not affect the tritium distribution.

We also produced a metalized capacitor pattern on wafers with tritium-containing oxides. These capacitors were heated to 350°C for 20 minutes with some having +30 V applied to the metal and others having -30 V applied to the metal. The metalization was then etched away and autoradiographs were prepared. These autoradiographs show the metalization pattern but do not show any effect of the applied bias. We interpret this to mean that a significant amount of tritiated water diffused out of the oxide from regions not covered by metal. The observation that the applied bias had no influence on the distribution of tritium indicates that very little of the tritium is ionized.

Others have done similar work with tritium[15,265,267]. They also find that applied voltages do not significantly influence the tritium distribution. Burkhardt[265] recently reported that oxides prepared in tritiated steam could subsequently be baked in dry oxygen at the oxidation temperature to remove all traces of tritium.

6.6 Preparation of Oxides With an Optimum Water Content

Our work has shown that the absorption of a small amount of water substantially reduces the density of trapping states in thermally grown oxides. Our best thermally grown oxides were obtained in a 2-1/2" diameter oxidation tube with a flow rate of 2 ft^3/hr of dry (<15 ppm water) oxygen. After the oxidation we pull the sample to within 3" of the end of the tube in 2 seconds. The sample is taken from the tube about 5 seconds later.

7. CONCLUSIONS AND RECOMMENDATIONS

7.1 Conclusions

MOS transistors are well suited for complex high density circuitry in electronic systems for space applications. This twelve-month program combined experimental investigations and a search of the available pertinent literature to develop a better understanding of the causes of instability, high threshold voltage and the radiation sensitivity of MOS transistors and to develop improved MOS transistors.

7.1.1 Instability

During this program all of the known types of instability were studied and the causes were largely delineated. The results of this effort should make it possible to devise methods to prevent unstable devices from being used in space applications.

1. During this program, published information appeared that shows that sodium contamination is a chief cause of the instability observed in MOS devices at elevated temperatures. Radiochemical techniques show that a phosphorus glass layer getters sodium from the oxide layer. If the phosphorus glass layer is too thick it can cause an instability due to its own polarizability.

2. Our experimental work has shown that practical device-fabrication techniques which were designed to minimize the sodium contamination in the oxide layer can be used to prepare oxides having alkali ion densities below 5×10^{10} cm^{-2}.

3. Another type of mobile ion instability is observed at room temperature especially after an MOS structure has been heated under a positive bias. This type of instability was observed at various times during the past several years but was considered to be of lesser importance than that due to sodium. This type of instability has also been reported in the literature and appears to be dependent on some unknown factor in each particular processing environment. The amount of this type of instability was found to be lower in samples made later in the program but the reason for the decrease could not be identified. Probably some unknown material in minute quantities plays a catalytic role in the interaction involving the oxide, the aluminum, alkali atoms, and water or hydrogen. This instability has been found

to be increased by a heat treatment of the metalized oxide. The level of instability is often increased by etching and rinsing of the oxide before the metalization. We have shown a capability to fabricate MOS devices having a density of this type of ions below 10^{10} cm^{-2}.

4. Slow traps cause an instability opposite in polarity to that due to mobile ions. This type of instability is not very troublesome in thermally grown oxides. Vapor plated oxides have slightly more slow traps than do thermally grown oxides. Our vapor plated silicon nitrides have many more traps than do our oxides.

5. Mobile charge and slow trapping coexist in the same sample. Feasibility has been shown for a technique in which C-V measurements, taken on an oxide after drift treatments at differing bias voltage levels and temperatures, are compared to at least partially separate the effects of mobile charge and trapping.

6. Surface ions are another source of instability, especially when the package is not hermetic. This was demonstrated in the experimental part of this program.

7. It appears to be impractical to stabilize oxides by drifting ions to the oxide surface and to remove them by etching away a thin layer of oxide. The sodium atoms in an oxide are not all ionized and apparently even if all of the ionized sodium atoms are removed more of the unionized atoms subsequently become ionized.

7.1.2 Threshold Voltage

The speed of MOS transistors can be increased and the required operating power can be decreased if the threshold voltage is reduced. The threshold voltage can be reduced by decreasing the immobile charge density in the oxide. The threshold voltage is also affected by traps at the oxide-silicon interface because these traps immobilize carriers. Alternatively, one might utilize the capability to reduce the immobile charge density to fabricate transistors with a given threshold voltage but with thicker oxides to increase the oxide breakdown strength. Transistors having a higher breakdown strength are less likely to be damaged by accumulated static charge during routine handling of the devices.

8. A number of techniques were experimentally developed on this program by which oxide layers were fabricated having lower densities of immobile charge. It was shown that the immobile charge density in either thermally grown or vapor plated oxides is strongly dependent on the crystalline orientation of the silicon. Vapor plated oxides, made with CO_2, have substantially lower immobile charge densities than do thermally grown oxides on silicon having the same crystalline orientation. A reduction in the temperature (from 1200° C to 1000° C) used for thermally oxidizing silicon yields a lower immobile charge density. A treatment involving an electroless nickel plating on the back of the oxidized wafer and a subsequent heat treatment significantly reduces the immobile charge density. A heat treatment at 300° C for 1 hour reduces the immobile charge density in thermally grown oxides.

9. On the other hand, another process (using $SiH_4 + O_2$) for vapor plating oxides did not yield lower immobile charge densities. Oxides grown thermally at 1200° C in diluted oxygen had a higher immobile charge density than oxides grown in pure oxygen. A phosphorus-doped vapor plated oxide had a higher immobile charge density than similar vapor plated oxides without phosphorus doping. Heat treatments at higher temperatures (400 to 1200° C) in moisture- or hydrogen-containing ambients increase the immobile ion density.

10. It is feasible to make p-channel MOS transistors that have lower threshold voltages by using silicon wafers cut on the ⟨100⟩ planes instead of on the ⟨111⟩ planes. The trap density is not adversely affected by this change.

11. Efforts to build p-channel MOS transistors with vapor plated oxides yielded devices having relatively high threshold voltages. These devices had a higher immobile charge density than that we found in vapor plated oxides in capacitor structures. The threshold voltages of these devices were also influenced by trapping. Our finding that vapor plated oxides can be made to have low immobile charge densities in capacitor structures and the finding recently reported in the literature that such vapor plated oxides have low trapping densities give us cause for optimism that further work will show that vapor plated oxides can be used to build MOS transistors with lower threshold voltages.

7.1.3 Radiation Resistance

The advantages of MOS transistors can be most fully utilized

when means are found for improving their resistance to radiation in non-optimum space environments.

12. The most sensitive effect of gamma radiation on MOS transistors is an increase in the threshold voltage due to the ionization of traps in the oxide. The transconductance is decreased somewhat because of either the formation or the activation of carrier immobilizing traps. The leakage currents are hardly affected by irradiation doses that cause the changes in the threshold voltage and transconductance.

13. In our experimental work we found several groups of MOS devices that were relatively resistant to radiation. A group of p-channel MOS transistors, which had a phosphorus deposition, a heat treatment and a subsequent partial removal of the oxide, was more resistant to radiation under either a positive or a negative bias. Another group of p-channel MOS transistors, made by another manufacturer, showed a radiation-induced reduction in threshold voltage during an irradiation with a negative gate bias. Data indicate that oxides that are thermally grown at 1000° C exhibit more resistance to radiation than similar oxides grown at 1200° C. Devices made with silicon nitride are substantially more resistant to radiation than those made with oxides. The reasons for these differences are not yet understood.

14. There appears to be no difference in radiation resistance between thermally grown oxides and vapor plated oxides, and between oxides grown on ⟨111⟩ and ⟨100⟩ oriented silicon. The radiation resistance does not depend on the mobile ion content in the devices, on a nickel treatment, on the dryness of the oxide or on the ambient temperature during the irradiation.

15. The radiation resistance does not differ for capacitors made on n- or p-type silicon when they are irradiated at the same applied voltage. However, since the applied gate voltage on n-channel MOS transistors is more likely to be positive than it is on a p-channel MOS transistor, one should expect p-channel transistors to be more resistant to radiation.

16. A physical model exists that permits one to explain the observed effects of radiation on MIS (metal-insulator-silicon) devices, particularly the observation that devices degrade much more rapidly during an irradiation under a positive voltage than under a negative voltage.

7.1.4 Other Considerations

The value of the information collected in this program extends beyond the field of MOS devices to such areas as bipolar devices and circuitry, devices using insulating layers other than oxides, and to the behavior of water in thin oxide layers.

17. The literature review conducted during the program provides a good basis for further work in the MIS field.

18. MOS studies have provided an improved understanding of carrier trapping and generation-recombination at the silicon surface. This understanding along with the MOS analytical techniques for measuring the silicon surface properties will be valuable in the development of bipolar devices for operation at very low operating power levels.

19. The understanding of the causes and effects of immobile and mobile charge, of the various types of trapping and of the effects of radiation in MOS devices can be extended to improve both MOS and bipolar microcircuits. MOS analytical techniques and the understanding of metal, insulator and silicon surfaces and interfaces made possible by the development of MOS devices will be of great value in efforts to improve the reliability, the stability and the performance of all types of microcircuits.

20. Water was not absorbed in significant amounts by the oxides studied at temperatures below approximately 300° C. This indicates that the diffusion constant in these oxides is similar to that in fused silica. Above this temperature, trace levels of water very strongly alter the density of states. Water has not been found to significantly affect the immobile, or mobile charge density. Tritium tracer experiments indicate that very little of the tritium in the oxide is in ionized form. To obtain the optimum combination of a low immobile charge density and a low density of trapping states we found it necessary to prepare our thermally grown oxides in dry oxygen (<15 ppm water) and then to cool the sample at the gas outlet end of the oxidation tube so that a small controlled amount of water was absorbed by the oxide from the room air.

7.2 Recommendations

Future work should be aimed at translating the information accumulated in this program into practical devices having improved capabilities for use in space hardware.

1. We recommend that the techniques by which the immobile charge density can be reduced be used to build transistors with thicker gate oxides to increase the breakdown voltage of the gate oxides, and thereby to reduce the probability that these oxides are damaged by static charge during handling of the devices.

2. The reproducibility of lower transistor threshold voltages should be evaluated, since their utility depends on their reproducibility.

3. Additional evaluation should be made of the feasibility of building MOS transistors with lower threshold voltages by means of the techniques that were shown to yield lower immobile charge densities in MOS capacitor structures.

4. We recommend that the effectiveness of the process involving a phosphorus deposition, a heat treatment and subsequent partial oxide removal for reducing the effects of radiation on MOS transistors be evaluated further.

5. The observation that some transistors improve during an irradiation with a negative bias calls for further study.

6. A research effort should be undertaken to establish more clearly the causes of various kinds of states, and to separate and characterize the various kinds of states that are now known to affect MOS transistor threshold voltage and transconductance, bipolar diode reverse current, and bipolar transistor current gain.

7. We recommend that MOS techniques be used to analyze problems in both bipolar and MOS microcircuitry and that the treatments for controlling the surface potential and state densities be used to improve microcircuit performance and stability.

APPENDIX A

LITERATURE REVIEW AND CORRELATION OF PUBLISHED INFORMATION

Introduction

The growth and development of the semiconductor device industry has been strongly dependent on the understanding of semiconductor surface properties. The development of device designs and processing techniques that best use or reduce the effects of these properties has played a major role in the history of semiconductor devices.

Early Field Effect Transistors

In 1948, Shockley and Pearson[203] fabricated a structure with a thin insulating sheet between a germanium sample and an evaporated metal film. They measured the change in conductance of the germanium as a function of the voltage applied to the metal. They found that only approximately 10% of the charge induced in the germanium was mobile. They postulated that the rest resided in bound states on the germanium surface.

In 1952, Shockley[204] devised the unipolar field-effect transistor in which he isolated the channel, which controlled the

conductance, from the carrier-immobilizing surface states by means of depletion layers formed at the surfaces. However, this device had the disadvantage that it could only be operated in the depletion mode. At about the same time, the invention of the bipolar transistor (a device in which the active region was located within the semiconductor so that surface properties were less important) overshadowed the work on field effect transistors.

Passivation of Bipolar Transistors

During the 1950's, large numbers of germanium transistors were produced in which acceptable surface properties were achieved by empirically developed processing techniques. To protect these transistors from severe surface problems, they were packaged in hermetically sealed packages containing very carefully controlled ambients.

In 1959, Atalla et al.[6,7] studied the silicon-silicon dioxide system where the oxide was produced by thermal oxidation, and found that such an oxide produced stable and reproducible surface properties. Combining this knowledge with an earlier finding[54] that SiO_2 can be used as a diffusion mask to form device structures, planar silicon transistors and diodes were invented[84].

These planar devices were found to have improved electrical characteristics in those parameters (or at those operating points)

for which the surface effects (at the edge of the junction where the junction meets the surface) were significant. Such improved parameters include I_{CBO}, noise figure, and h_{FE} at low currents.

However, even though oxides make the silicon much more insensitive to the ambient gas, ionic drift in the fringing electric field at the periphery of the junctions induces changes in the distribution of the surface potential and thereby causes the electrical characteristics to drift[6].

Metal-Oxide-Silicon Devices

In 1960, Kahng and Atalla[104] proposed a silicon structure in which an insulated gate was used to induce conduction between two diodes. The theory of this device was developed by Ihantola[98] in 1961. In 1962, Hofstein and Heimann[74,85] described a metal-oxide-semiconductor, or MOS, field-effect transistor with an insulated gate on single-crystal silicon. The improvements in surface characteristics made possible by oxide passivation made it possible to build these field effect devices so that the trapping of charge was relatively less important. These insulated gate devices have the desirable feature that, unlike the junction unipolar field effect transistor, they can be operated in either the enhancement or the depletion mode. Many papers[232-234] have appeared, describing a variety of useful applications for this device and noting its advantages:

1. Very high input impedance,
2. Functions with signals of either polarity,
3. Low noise level at high frequencies,
4. Simplifies circuit design,
5. Relatively insensitive to temperature,
6. No carrier storage,
7. No offset voltage,
8. Ease of fabrication,
9. Larger packing densities, possible because no isolation is necessary between components and because MOS transistors can be used as resistors.

It was originally predicted[232,233] that field effect transistors, being majority carrier devices, would tolerate radiation up to a level where there is a change in the mobility or in the density of donor or acceptor centers, that is, up to a level about ten times the dose at which lifetime degradation begins. On this basis, field effect transistors were expected to tolerate a radiation dose approximately ten times greater than bipolar transistors of comparable dimensions. However, it has since been shown[12,93,94,116,188,217,222] that the effect of radiation on the oxide layer begins at a level well below that which directly affects the silicon. For this reason, MOS devices are sensitive to much smaller doses of radiation than are bipolar devices.

The oxide and oxide-silicon interface properties play a very important role in determining MOS device performance, stability, and reliability. Because the oxide between the gate electrode and the channel is very thin (only 1000 to 2000 Å), even a small applied voltage sets up a strong electric field, which causes motion of ions in the oxide and produces undesirable effects on the device characteristics. For example, only four volts applied to the gate of a 1000-Å thick oxide produces an electric field of 10^5 V/cm. This high field drifts any mobile ions in the oxide, especially at higher temperatures. Since the oxide layer is so thin, ions can very quickly drift from one face of the layer to the other. This changing distribution of charge in the oxide induces undesirable drift in the electrical parameters of the device.

A further problem arises because even if the charge in the oxide is immobile, and does not cause drift in the device characteristics, it causes a transistor to have a threshold voltage level different from that desired by the circuit designer. This level of threshold voltage results from the fact that immobile charge in the oxide affects the surface potential of the silicon. This undesirable charge causes a p-channel MOS transistor to require a higher voltage than desirable to induce channel conductance, and causes an n-channel device to conduct even at zero gate-to-source voltage.

The presence of trapping or recombination centers along the oxide-silicon interface also plays an important role in determining the electrical characteristics of MOS devices. Trapped charge is immobilized and does not contribute to channel current, and therefore trapping reduces channel conductance and transistor transconductance. The transistor threshold voltage, that gate voltage which brings the channel to the threshold of conduction, is, therefore, increased by trapping.

The presence of recombination centers provides a source of leakage current at the drain-substrate diode. In bipolar devices, recombination centers are a source of junction leakage current, and they reduce beta due to recombination of carriers in the base region.

Literature Describing Surface-Related Physical Principles of MOS Devices

MOS device descriptions and design equations have been presented by a number of authors, including those of references 22, 50, 76, 82, 85, 98, 99, 139, 156, 162, 195, 225, and 233.

The physics of MOS devices has been well presented in many papers (references 22, 50, 76, 82, 85, 98, 99, 139, 156, 162, 195, 225, 233 and 261).

These papers give extensive coverage to the theory of MOS device operation, including the dependence of transistor transconductance on geometry, the frequency dependence of the capacitance on the transconductance, and the basic dependence of the capacitance on conductance of the layer in the silicon near the surface on the applied voltage or on charge in the oxide. It is this last area with which this program is concerned, and because of its importance, the review of the effects of applied voltage and oxide charge has been placed in the introduction to this final report.

Fabrication of MOS Devices

On the basis of published information relating to the fabrication of MOS structures, the following outline gives the typical important processing steps involved.

1. Prepare silicon wafer for oxidation by a series of cleaning and etching operations.
2. Oxidize the wafer to a thickness of about 6000 Å.
3. Photolithographically cut openings in the oxide to delineate the mask pattern in preparation for diffusion of the source and drain regions.
4. Diffuse the source and drain regions.
5. Remove oxide from the back of the silicon; nickel plate and heat so that the nickel getters[100] metallic impurities from the silicon.

6. Photolithographically reduce the oxide thickness for the gate region and cut openings for the contacts to the source and drain regions.
7. Deposit the contact metal (usually aluminum) layer and etch (again using photolithographic processes) the layer to form the electrodes for the source, gate, and drain regions.
8. Heat treat the processed wafer to reduce the resistance at the electrode contacts.
9. Scribe the wafer, bond the chips to headers, bond device terminals to package terminals, and seal packages in a controlled ambient.

Due to the sensitivity of the device parameters to minute differences in the condition of the oxide, those processes which affect the oxide condition are the most critical steps in the fabrication sequence.

Oxidation Processes

Thermal Oxidation. In 1957, Frosch and Derick[54] found that silicon surface can be oxidized to form a mask for the diffusion steps which form the various regions of a transistor structure. Atalla et al.[7] demonstrated that the oxide passivates the surface, making the underlying device comparatively insensitive to the

ambient gas, and thereby stabilizes the electrical parameters of the device. At the 1960 Electron Devices Meeting, Hoerni[84] showed how the masking and passivating properties could be combined to make planar transistors and diodes.

Ligenza and Spitzer[130] studied the mechanisms involved in the thermal oxidation of silicon by preparing oxides using combinations of O^{16} and O^{18} isotopes. By measuring the infrared transmission through these oxides as a function of oxide layer thickness as the oxide layer was etched away, they were able to determine that the diffusing species during oxidation is oxygen. They noted that an oxygen exchange occurred during the oxidation process at a rate at least as fast as the rate of growth. They inferred that the actual oxidation and the rate limiting process take place at the silicon-oxide interface. Pliskin and Gnall[177] used a selective etch technique that also showed that the oxidation takes place at the silicon interface.

Jorgenson[103] applied an electric field across the oxide during oxidation and showed that the dependence of the oxidation rate on the field strength and polarity is such as to indicate that oxygen ions are the predominant species diffusing through a growing oxide film. Goetzberger[60,62] recently showed that oxidation in an electric field can reduce the densities of charge in

oxides prepared by thermal oxidation in steam or wet oxygen. No influence of the field was found on the effective charge density in thermal oxides formed in dry oxygen. Schmidt[200] prepared sodium-free oxides that contain less than 10^{11} mobile charges per cm^2, as tested in steam at 300°C for 26 hours with a field of 10^6 V/cm, with the silicon biased negative.

Deal[31] studied the oxidation of silicon in dry oxygen, wet oxygen, and steam. Lukes and Schmidt[142] investigated the oxidation of silicon in dry oxygen. Fuller and Streiter[57] reported on similar work which substantiates the oxidation growth rates reported by Deal. Ligenza[132] studied the oxidation of silicon by high pressure steam (25 to 500 atmospheres). Lieberman et al.[129] studied the effects of water vapor pressure on the rate of thermal oxidation of silicon. Deal and Sklar[30] studied the oxidation of heavily doped silicon.

A good review article on the formation and properties of oxides on silicon was prepared by Donovan[33]. He discusses the kinetics of various oxidizing reactions and the results from typical experimental systems. He also describes several models for the accumulation of electrons near the surface of oxidized silicon.

Vapor Plated Oxides. Oxides have been vapor plated on silicon by several techniques. Jordan[101] and Klerer[109] reported techniques for thermally decomposing organo-oxy-silanes or alkoxysilanes to vapor plate SiO_2. Steinmayer and Bloem[218] developed a useful technique by which they successively vapor plated silicon and silicon dioxide in the same reaction chamber. Tung and Caffrey[230] discussed the deposition of oxide on silicon by the reaction of a metal halide with a mixture of hydrogen and carbon dioxide. MacKenna et al[143] used a similar reaction with $SiCl_4$ and CO_2. Peterson et al[175] reported on vapor plating done at 200 to 400°C to form oxides for passivating semiconductor surfaces. A combination of vapor plated and thermally grown oxides has been used[257] in forming bipolar transistors to improve the oxide masking process during the emitter diffusion and thereby improve the base-collector junctions. Further information on vapor plating can be found in "Vapor Plating" by Powel et al[186].

Other Oxidation Processes. A number of other processes have been studied for forming oxides on silicon which at the time of this writing have not found favor with the producers of MOS devices. Ligenza[133] has oxidized silicon in an oxygen gas plasma excited by a microwave generator.

Pliskin and Lehman[176] studied pyrolytically deposited films because of their lower deposition temperature. Such an oxide deposition leaves the silicon surface undisturbed. These considerations are important when there is concern about the changes that may take place in the silicon during oxidation. They developed a technique for densifying pyrolytically deposited films to improve their effectiveness as passivation layers and diffusion masks.

Valletta et al[231], and Fuller and Baird[56] formed films by reactively sputtering a silicon cathode in oxygen. Ligenza and Povilonis[134] sputtered silicon through an oxygen plasma to form silica layers on silicon at substrate temperatures down to 25°C.

Schmidt and Owen[197] used a wet anodic process to form oxides at room temperature. Duffek et al[39,40] anodically oxidized silicon in ethylene glycol solutions. Dreiner[37] compared the dielectric properties, leakage currents and etch rates of anodically and thermally grown oxides prepared for MOS structures.

Tokuyama[227] formed a two-layer oxide in which the outer layer consisted of a mixture of PbO and SiO_2.

Alt et al[3] deposited silicon oxide at room temperature by decomposing an organo-silicon compound in a low energy gaseous atmosphere created by electron bombardment.

Pliskin[180] deposited SiO_2 using a technique in which he evaporated the SiO_2 with an electron gun.

Other Insulation Layer Possibilities

Silicon nitride has received some attention as a possible alternative material to the oxide in metal-insulator-silicon devices. The dielectric properties of silicon nitride were studied by Barnes and Geesner[10]. Hu[92] investigated a wide range of physical properties of silicon nitride. Fa et al[46] used silicon nitride for the isolation layer in microcircuits. Doo[35] presented data on the properties of silicon nitride as a diffusion mask for silicon diffusants, and Doo and Jones[36] discussed its use for isolation layers in integrated microcircuits. Tombs et al[228,229] have used silicon nitride for the insulation layer in insulated gate field-effect silicon transistors. References 144 and 248 are further evidence of recent attention given to silicon nitride.

Techniques for Evaluation of Oxides

Various experimental techniques have been used to evaluate and study the properties of oxides that are described in the literature. Some of these are discussed below.

Capacitance-Voltage Relationship. One of the most useful techniques for studying the properties of oxides involves the measurement of

the capacitance of MOS capacitors as a function of such variables as the applied d-c voltage, the measurement frequency, or the temperature.

Terman[225] and Lehovec et al[123] measured the capacitance of MOS capacitors as a function of the applied d-c voltage and the measurement frequency. They made an effort to locate allowed energy levels in the energy gap and to evaluate the associated time constants.

Grove, Snow, Deal and Sah[28,67,69,70] published a number of papers that demonstrate how C-V characteristics may be used to study a wide variety of oxide-related properties, including the distribution and movement of charge in the oxide, the redistribution of dopant atoms in silicon during thermal oxidation, and the effects of charge in the oxide on the electrical characteristics of p-n junction diodes that intercept the silicon surface under the oxide.

Dunavan and Lawrence[41] tested oxides before metalization by using a gold ball probe as a temporary metal electrode on the oxide.

Lehovec and Slobodskoy[124] calculated the dependence of the impedance of MOS capacitors on bias voltage, frequency, and substrate resistivity for a semiconductor free of surface states.

Sprague et al.[215] studied oxide properties in MOS capacitors with the emphasis on the properties desired for good capacitors -- permittivity and loss tangent.

Zaininger and Warfield[252] recently discussed the limitations of the MOS capacitance method for the determination of semiconductor device properties.

Lehovec et al.[125] used a capacitor with a large circumference-to-area ratio to study the migration of charges in the region surrounding the metal electrode of an MOS capacitor.

Heiman et al.[75] and Clark[26] discussed ways to determine the conductivity type of the silicon in MOS devices.

Conductance Measurements. Hofstein[88] showed that the measurement of channel d-c conductance of an MOS transistor has an advantage over capacitance measurements in that faster response times can be measured.

Goetzberger[61] developed a technique using a ring-dot structure that permits measurement of the conductance of inversion layers under oxides which have not been subjected to the diffusions necessary for a MOS transistor structure.

Other Measurements. Shockley et al.[205,206] used surface potential measurements to study charge motion over the surface of the oxide.

Yamin[245] investigated the d-c current properties of oxides. Such measurements permit the study of various kinds of electrolytic effects, charge storage, and rectification at boundaries.

Green and Nathanson[64] used a scanning electron microscope to observe inversion layers under insulated gate electrodes.

Pliskin and Lehman[179] evaluated structural differences, density, porosity, refractive index, and passivation efficiency by means of infrared absorption spectroscopy, preferential etch procedures, and a technique known as VAMFO (Variable Angle Monochromatic Fringe Observation)[178].

Infrared transmission measurements can be used[1] to determine the presence of "water" in the form of OH groups in fused silicon.

Rosier[194] made a special diode structure to measure the surface recombination velocity beneath an oxide as a function of the voltage applied to a metal electrode on the oxide.

Grove and Fitzgerald[70] introduced sodium ions into the oxide covering a p-n junction to create higher fields. This enabled them to show that anomalous channel currents are due to a breakdown mechanism in the channel.

To study the distribution of traps, Schroen[201] used a spot of light to create non-equilibrium carriers in small local areas to affect the breakdown voltage of p-n^+ junctions and MOS structures.

Kerr[107] has made a comparative evaluation of four methods for measuring ionic conduction in passivation films: C-V stability, charge-time measurement, current-voltage loop, and charge-temperature measurement.

Klein and Gafni[108] studied the maximum dielectric strength of thin silicon oxide films.

Model for Oxide Structure .

Glasses The oxide on oxidized silicon is amorphous SiO_2. It is in the glasslike or vitreous state, a state believed to be a solid with the disorder of a liquid frozen into its structure. Although the history of man's work with glass spans a greater time than his work with most other materials, there still is disagreement over the theory of glass structure.

The first real advance in the theory of glass structure was due to the development of the random network theory which describes glass as lacking the symmetry and periodicity of the crystalline state. In a competing theory, glass is assumed to contain microscopic crystals with definite stoichiometric compositions joined together by amorphous zones. More detailed discussion of glass structure may be found in references 90 and 240. A number of simple rules have been proposed for relating the way oxygen anions and silicon cations link together for an oxide to exist in the glassy state. Briefly, the rules state that glass-forming cations (e.g., B^{3+}, Si^{4+}, P^{5}) are surrounded by polyhedra of oxygen ions in the form of triangles or tetrahedrons. The oxygen ions are of two kinds: bridging oxygen ions, each of which link two polyhedra; and nonbridging oxygen ions, each of which belongs to only one polyhedron. Such a system has a polymer

structure with long chains cross-linked at intervals. In such a structure, there are regions of unbalanced negative charge where the oxygen ions are nonbridging. Cations of low positive charge and large size (Na^+, K^+, Ca^{2+}) may exist in holes between oxygen polyhedra where they compensate the excess negative charge of the nonbridging oxygen atoms.

Some cations of large charge and small size may isomorphically substitute for silicon ions in the structural network of the glass. Oxides forming the basis of a glass are called network formers, and those which are soluble in the network are network modifiers.

It has been established that glasses can be formed of B_2O_3, SiO_2, GeO_2, P_2O_5, As_2O_5, As_2O_3, and Sb_2O_3. Possible glass formers include V_2O_5, ZrO_2, and Bi_2O_3. Oxides of Ti, Zn, Pb, Al, Th, and Be apparently do not form glasses, but they modify certain properties of glass. Oxides of Sc, La, Y, Sn, Ga, In, Mg, Li, Ba, Ca, Sr, Cd, K, Rb, Hg, and Cs may act as network modifiers.

Stevels and Katz[219] have discussed the wide variety of possible imperfections that might exist in the SiO_2 network. The following is a list of the imperfections they describe, along with their opinions concerning the abundance of each type.

Silicon Vacancy	- Silicon vacancies are not likely because of the very high bonding energy with oxygen.
Oxygen Vacancy	- Oxygen can exist either in bridging or in nonbridging positions in the lattice. Nonbridging oxygen atoms can break away from the lattice, leaving oxygen vacancies.
Interstitial Silicon	- Interstitial silicon is unlikely because of the strong tendency to bond with oxygen.
Interstitial Oxygen	- Nonbridging oxygen atoms exist as a part of the Si-O network. Under certain special circumstances, interstitial oxygen exists which is not a part of the network.
Replacement of Silicon by Another Cation	- The replacement of silicon by cations (Al^{3+}, B^{3+}, P^{5+}) is very common.

Replacement of Oxygen by Another Anion	- This possibility should not be overlooked, but does not seem to occur to any important extent.
Interstitial Cations Other Than Silicon	- Interstitial cations in glasses and quartz crystals are very common.
Interstitial Anions Other Than Oxygen	- This occurrence is unlikely, by may be possible in special circumstances.

Silicon Oxide · Donovan[33] has written a review paper on the properties of oxides on silicon. He notes that silica glass is thermodynamically unstable below 1710°C and should devitrify to a stable crystallized form. However, the rate of devitrification is negligible at temperatures below 1000°C. Silicon ions, due to their large charge, cannot move without breaking four oxygen bonds. Oxygen ions, on the other hand, are freer to move through the lattice, since bridging oxygen ions are bound to only two silicon ions, and nonbridging atoms to only one. A network modifier, when introduced as an oxide, ionizes and gives up an oxygen atom to the network. The modifier metal ion occupies an interstitial position in the network and the oxygen ion enters the

network, producing two nonbridging oxygen ions where formerly there was one bridging oxygen ion. The network is weakened, as manifested by a lower melting point.

The water content of silica glass is regarded as an important factor in determining its properties. Drury and Roberts[38] have determined the solubility and diffusion constants for water vapor in silica glass by use of tritiated water. Moulson and Roberts[159] used infrared absorption data to study the diffusion and solubility of water in silicon glass. Water vapor can enter the silica glass network either as hydroxyl ions or molecular water, or both. The hydroxyl ion can also be formed by the attachment of hydrogen ions to nonbridging oxygen atoms, producing a tightly bound stable hydroxyl ion, or it may be formed in less stable configurations by other hydrogen-silica reactions. The presence of hydroxyls in silica glass tends to weaken the structure by breaking oxygen bonds and replacing them with single-bound hydroxyl ions. The effect is analogous to changing bridging oxygen ions to nonbridging oxygen ions. Donovan further reports that when divalent ions, such as Ca^{++} or Sr^{++} are introduced to silica, the mobility of alkali ions in the silica decreases.

Garino Canina and Priqueler[58] have found the drift of "water" in an electric field in pure fused silica to be dependent on the presence of aluminum.

Revesz[190] reviewed the structure of grown silicon dioxide films from the viewpoint of a physical chemist. The defect structure is shown to influence many of the phenomena observed in MOS devices. This defect structure is quite sensitive to variations in oxide growth techniques and to the thermal and ambient gas treatments following the formation of the oxide. According to the proposed model, thermal growth of silicon dioxide proceeds through the migration of oxygen interstitials which act as acceptors. The presence of water in the oxidizing ambient, an aftertreatment in hydrogen, or some reactions with the gate metal introduce a donor state in the forms of trivalent silicon. Besides the relationship between defects and oxide growth, Revesz discussed the interactions between the silicon and its oxide, reactions at the gate-oxide interface, and the effects due to an inhomogeneous distribution of defects.

Seraphim et al[202] studied the effects of chemical additives and of annealing procedures, and have listed some of the electrochemical reactions that might take place within the oxide.

Semiconductor-Oxide Interface

Schmidt and Sandor[198] reviewed the state of knowledge concerning the semiconductor-oxide interface. They discussed how the various properties of the silicon surface change with thermal

oxidation of the surface. For example, oxidation may tie up dangling bonds at the surface and thereby reduce the density of fast states. On the other hand, states located within the oxide, which are not in intimate electrical contact with the silicon, are observed as slow states which are added during the oxidation.

Some of the important properties of the oxide-semiconductor interface can be predicted when the interface is treated as a heterojunction, as discussed by Lindmayer[136, 137].

Energy Band Diagram

Williams[243] experimented with the photoemission of electrons from silicon into silicon dioxide and was able to draw the energy diagram in Figure 1. Besides uncovering the energy relationships expressed in the diagram, he found traps in the oxide at a level more than 2 eV below the conduction band of the SiO_2. He found that he could fill these traps by irradiating with ultraviolet light and then empty them with visible light. The density of traps was 3×10^{14} cm^{-3}, with a capture cross section of 10^{-12} cm^2. The mobility of electrons in the oxide is 20 to 40 cm^2 per volt-sec.

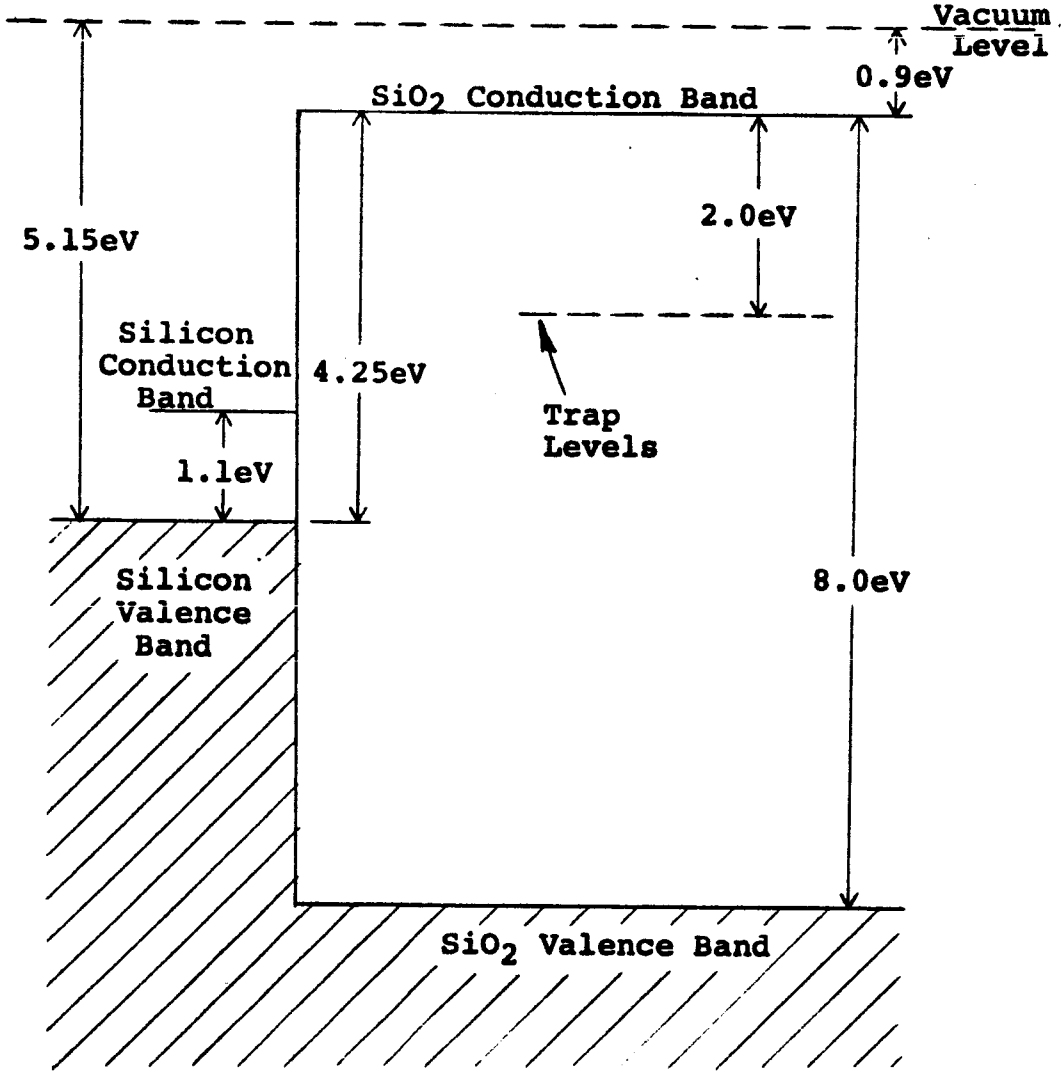


Figure 1. Energy band diagram for the interface between silicon and SiO_2.

Mobile Charge

Instability of device parameters has been one of the most important problems associated with MOS devices. The basic cause of device instability is the instability in the charge distribution in the oxide layer. This instability is due to any of three main effects. Alkali ions such as sodium or lithium can drift or diffuse through the oxide at temperatures such as 200 to 300°C. Some species of charge (probably protons) related to hydrogen or water move through the oxide quite easily at room temperature. Traps existing in the oxide near the silicon interface can change their state of occupancy and thereby affect the density of charge in the oxide.

The literature concerning the motion of charges through SiO_2 is extensive. Owen and Douglas[170] examined the d-c electrical conductivity of various samples of fused silica and found it to depend particularly on the sodium concentration. The d-c conductivity was reported to be substantially independent of the water content, whereas the dielectric properties were said to be almost entirely determined by the water content. The nature of d-c conductivity is further discussed by Owen.[171]

Proctor and Sutton[187] have studied the motion of ions in glass. The observed behavior agrees with a model in which cations are mobile but anions are not.

Collins[27] explained the electrochemical behavior of oxide films on silicon in terms of the migration of protons.

The electrolysis of vitreous silica and the equilibria of hydrogen or water and silica are discussed in references 11, 42, 79 and 80.

Lee[119-121] has extensively studied the diffusion of hydrogen in fused silica and has discussed the role of the hydroxyl in this connection.

Snow et al[207] developed a model for the motion of ions in oxide films of MOS devices. Alkali ions were intentionally deposited at the metal oxide interface and their motion through the oxide was studied as a function of time, temperature and applied voltage. They showed that alkali ions are capable of creating the type of instability that has been a problem in MOS devices. Their paper also includes a model for explaining the observed characteristics of the instability.

Logan and Kerr[140] used a different technique to introduce alkali ions into the oxide and substantiated the findings of Show et al[207].

Yon, Kuper, and Ko[248, 249] used the techniques of radiochemical analysis to carefully study the behavior of sodium in oxide layers. They used neutrons to activate the sodium and then measured the activity as successive etches removed thin layers of

the oxide. They were able to find good correlation between the sodium content in the first 1000 Å of oxide adjacent to the silicon and the position of the flat band voltage of the C-V characteristic curve. They correlated the drift in sodium atom distribution with the observed change in this voltage. They detected small differences between the cases in which sodium was introduced as NaOH, NaCl, and NaBr. In the case of NaBr, they found that the sodium concentration increased near the silicon interface, while the C-V surve shift indicated a decrease in ion concentration. They studied how the impurities were redistributed by different conditions of bias voltage and temperature. They found, in support of earlier work by Snow et al[207], that the sodium segregates toward the oxide interfaces with the metal and the silicon. They showed that when sodium is deliberately introduced into the oxide by diffusion, not all of the sodium is ionized. They further demonstrated that a phosphosilicate layer on the oxide getters the sodium; i.e., sodium segregates to it and is held in it.

Similar work involving radiochemical techniques done by Brown et al[14] and Carlson et al[19] substantiates many of these findings.

It had been suggested[202, 226] that oxygen vacancies are capable of the type of ionic motion that causes MOS device

instability. Collins[27] suggested that this is hardly consistent with the observed values for the diffusion constant and activation energy.

Kerr et al[105] have shown that a phosphosilicate layer on an oxide produces a stabilizing effect on the electrical characteristics of the silicon oxide.

Brown et al[14] and Chetney and Holschwandner[25] reported similar results.

Snow[208] reported that the stabilizing effect of a phosphosilicate layer occurs only if the thickness of the phosphosilicate layer is thin compared with the over-all thickness of the oxide.

Pliskin[183] studied the effect of phosphorus on SiO_2 by means of infrared spectroscopy and reported that there appears to be an increase in polymerization of the SiO_4 tetrahedra leading to a more dense structure which may retard the diffusion of impurity ions through the oxide film.

Yamin[246] found that a diffusion of boron into a phosphorus stabilized oxide destroys the stabilization, while even a light phosphorus diffusion over a boron diffused oxide restores the stability.

Hofstein[88] showed that in alkali ion-free oxides, ions suspected of being protons can be moved from the silicon toward

the metal at a rate up to five orders of magnitude faster than movement from the metal toward the silicon. This, he postulated, is due to traps at the metal-oxide interface. The true charge mobility in the oxide is that represented by motion toward the metal.

Burgess and Fowkes[15] used tritium to study the behavior of water or protons in silicon oxide.

Hofstein[88,89] and Gregor[65] show that the treatment of the oxide surface just prior to metalization plays a strong role in determining the magnitude of the mobile ion instability. Gregor[65] reported that the substitution of gold metalization for aluminum reduced the amount of such instability considerably.

In addition to the motion of charge through the oxide in a direction normal to its plane, it has been shown[12,151,173] that charges can move on the surface of the oxide to degrade the device properties. The motion of surface charge on the oxide was described as the mechanism responsible for the failure of Telstar. Shockley et al[205,206] used a Kelvin probe to show that motion of charges along oxide-covered silicon surfaces can form channels and/or change the device characteristics.

Immobile and Trapped Charge

The threshold voltage of MOS transistors is dependent on two basic parameters -- the density of immobile charge in the oxide or at the oxide-silicon interface that influences the surface potential of the silicon, and the density of trapping states in the silicon or oxide-silicon interface that trap and immobilize carriers that would otherwise contribute to channel current.

The influence of immobile oxide charge on threshold voltage has led many investigators to study the effects of various materials and treatments on the density of immobile charges. It has been found by most experimenters that the immobile charge density in thermally prepared oxides on <111> oriented silicon is 2 to 3 x 10^{11} charges/cm^2. Recently, Delord et al[32], Balk et al[9], and Miura[154] have reported that the immobile charge density is strongly dependent on the crystalline orientation with <111> yielding the highest density of immobile charges and <100> the lowest.

Lehman[122] conducted a series of experiments to determine the effect of the choice of metal on the surface conduction properties of MOS transistors. He also discussed the effects of heat treatments and various ambients.

Zaininger and Warfield[251] show that heating MOS capacitors at temperatures from 200 to 350°C for 5 minutes in hydrogen increases the negative surface potential under the oxide surrounding a metalized capacitor without changing the surface potential beneath the metal. The surface potential did not recover after baking in dry argon for two hours at 350°C. This indicates that the activation energy for removing the hydrogen is much higher than that for introducing it.

Balk[8] studied the effects of hydrogen at 320°C. He concluded that the main effect was the annihilation of fast states. He found a similarity between the effects of H_2 and those in oxides covered with aluminum.

Kooi[112] reported that the water content in the oxides very significantly determines the density of electron trapping states in the oxide. Thermal oxides prepared in wet oxygen have the fewest of such states, those prepared in dry oxygen have more, and those prepared with a phosphorus diffusion in a dry ambient have even more. This suggests that during the phosphorus diffusion the oxide becomes extremely dry. Low temperature heat treatments in hydrogen and water vapor decrease the density of these states. Kooi suggested that an aluminum electrode present

on the oxide during heat treatment can serve as a reducing agent for water present at its surface. Hydrogen atoms so formed diffuse through the oxide and react with trapping centers near the oxide silicon interface. He stated that it seems probable that the active states are related to unsaturated silicon bonds near the oxide-silicon interface which can lose their electron or hole trapping ability after they become saturated with hydrogen.

Further data on the effects of heat treatments in hydrogen can be found in the paper by Olmstead et al[168].

Cheroff et al[23, 24] reported that baking at 350°C yields improved transistor channel conductance. The involvement of the aluminum electrode was noted.

Revesz and Zaininger[191] discussed the influence of the oxidation rate and heat treatments on the surface state density. They mention that the presence of boron in SiO_2 is thought to facilitate the incorporation of hydroxyl through defect reactions.

Dunavan and Lawrence[41] used a gold ball probe to measure the surface state density after each step in the fabrication process. They found that the highest state densities are obtained by processes employing wet oxidation and/or slow cooling. On their samples, a treatment with P_2O_5 yielded a reduction in surface

state density (by a factor of 2.5) as well as an improvement in stability. They found that gold doping produced p-type surface states.

Goetzberger[62] has thermally oxidized silicon in an applied electric field. He found that the surface state density could be influenced by this technique in wet oxygen and steam-grown oxides, but not in those grown in dry oxygen.

Lindmayer et al[135,137] have analyzed the semiconductor-oxide interface in terms of a heterojunction model.

Seraphim et al[202] reported that a positive space charge can be developed in silicon surfaces when SiO_2 is doped with B_2O_3 and subjected to an electric field. Miura[154] found a slightly positive surface potential when he thermally oxidized in dry oxygen on <100> silicon and metalized with gold.

Trapping and Surface Recombination Effects

The development of oxide layers on silicon has provided a means for forming silicon surfaces with greatly improved surface recombination velocity. However, within the realm of thermally

grown oxides various experimenters have found wide differences in surface recombination velocity. Similarly, the density of traps and various kinds of allowed states have been found to depend on differences in minute quantities of foreign matter or on differences in oxide treatment.

The surface recombination velocity is a measure of the rate at which carriers can be created or destroyed at the silicon surface. This rate determines the leakage current at the drain-substrate junction of an MOS transistor.

Similarly, this rate determines the leakage current of a bipolar diode such as the collector junction of a bipolar transistor. Further, in a bipolar transistor, surface recombination removes carriers from the active region of the base and thereby degrades the beta of the transistor. This is particularly important at low operating current levels. The importance of this is illustrated by the wide divergence in the ability of various manufacturers to make bipolar transistors with good beta at low current levels.

The trapping of carriers is important in MOS transistors because carriers in the channel region cannot contribute to channel current. The presence of traps therefore degrades the transconductance of MOS transistors.

The effects of oxide traps on the MOS capacitance were discussed by Heiman and Warfield[78]. They show that traps cause hysteresis in the C-V curve of the type shown in Figure 2. The reason for this hysteresis is that slow traps within the oxide change their state of charge during the taking of the measurement. They conclude that very little information concerning the energy distribution and the capture cross-section of oxide traps is obtained from the analysis of MOS capacitance curves.

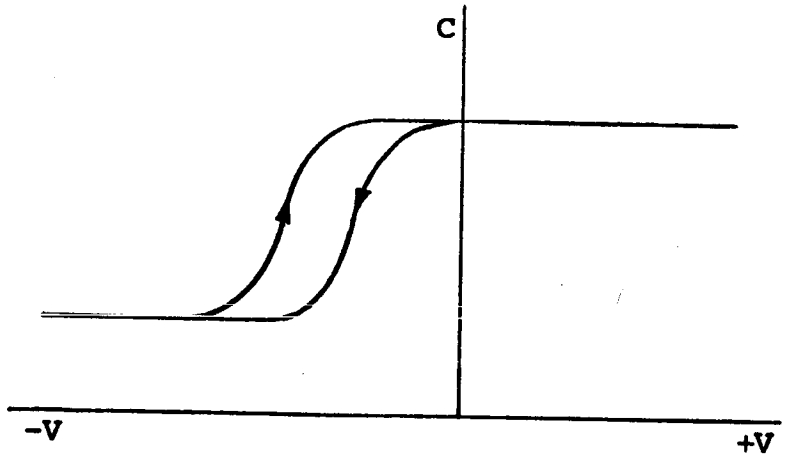


Figure 2. Effects of trapping on C-V curves.

Zaininger and Warfield[252] also investigated the effects of trapping on C-V curves. They studied the departure of the shape of the measured C-V curve from the theoretical curve to compute the trapping density. Their paper discusses the limitations of the capacitance measurement for the characterization of the traps.

Heiman and Miiller[77] measured the temperature dependence of the drain current of MOS transistors (at given drain and gate

voltages) and used the data to calculate the trapping or surface state density.

The negative temperature coefficient of the surface mobility of electrons in silicon causes the transconductance of transistors to decrease with increasing temperature. They showed that in some transistors, the transconductance increases with temperatures. This they attributed to the emptying of traps, and they developed this into a means for studying such traps.

Nicollian and Goetzberger[164] developed a technique for calculating the fast surface state density from measurements of the equivalent parallel conductance of the MOS capacitor as a function of the applied voltage. Traps cannot charge and discharge at the measurement signal frequency. The resulting inability of charge to flow on and off the capacitor is measured as a low Q for the capacitor. This reduction in Q can be used to study trapping densities.

Control rings have been used[21] to study the effects of surface potential on the impedance characteristics of p-n junctions.

Lehovec et al[123] and Terman[225] analyzed C-V characteristics as a function of bias and frequency to evaluate the properties of "surface states."

Schmidt[199] describes the effect of protons and alkali ions in oxide films on the surface recombination velocity. These impurities in the oxide are presumed to change the Fermi level in the oxide and thereby cause a charge transfer between the oxide and the silicon.

Fitzgerald and Grove[52,71] have described the mechanisms of channel current formation at p-n junctions.

Radiation Effects

Optimistic Predictions. It was predicted[232,233] that MOS transistors might be more tolerant of radiation than bipolar transistors because MOS devices are majority carrier devices. In this reasoning, the assumption was made that the failure mechanism would be either degradation of mobility or a change in the density of mobile charges.

Gamma Radiation. Unfortunately, when MOS transistors were tested by Hughes and Giroux[93,94,95,97] in a Co^{60} source, it was discovered that the transconductance of MOS transistors was severely degraded by exposure to 2×10^5 rads, even though the bulk conductivity and lifetime changes are negligible to absorbed dose levels of 10^6 rads. This degradation was attributed to ionization in the transistor by Compton electrons produced by the gamma radiation.

Hughes and Giroux[95] used an MOS structure to study the effects of ionizing radiation on the Si-SiO_2 interface. They found that the leakage current increase that caused the Telstar failure (which was explained by Blair[8] and Peck et al[173] as being due to ionization of the gaseous ambient and the subsequent drift of these ions in the fringing electric field at the edge of the junction) could be duplicated on devices in a vacuum of $<10^{-9}$ Torr.

Sonder and Templeton have studied the energy levels introduced in silicon under gamma radiation[210-212].

Kooi[111,113] has published a considerable body of data that shows the effect of ionizing radiation on MOS structures.

Fast Neutrons. Raymond et al[188] irradiated MOS transistors with fast neutrons up to 5×10^{14} NVT and found that the most significant neutron-induced parameter change is in the threshold voltage. Although they noted that comparison of the behavior of the MOS and the bipolar transistor is difficult because of the lack of good criteria, they concluded that MOS transistors have shown a potential advantage in radiation environments compared to junction and bipolar transistors.

Messenger[149] exposed MOS transistors to reactor neutrons and postulated that the neutrons produced displacement damage in the

form of positively charged oxygen vacancies in the oxide lattice or at the Si-SiO_2 interface.

Electron Irradiation. The effects of electron (1.5 MeV) irradiation on MOS transistors were examined by Stanley[217,260,275].

Szedon and Sandor[224] used low energy (10-16 KeV) electrons to irradiate MOS capacitors. They found that a positive charge was induced in the oxide and were able to remove it by annealing for fifteen minutes at 150 to 200°C. Speth and Fang[213] also report similar data.

Green et al[63] mention that electron irradiation with various electron energies can be used to study the location of damage sites that affect device parameters.

Flash X-Ray. Sullivan[222,223] and Long[141] have studied the effects of flash X-radiation and found the the principal effect is that of photocurrent in the drain substrate junction and gate displacement current which produces a change in gate voltage that in turn modulates the channel conductance.

Krueger and Griffin[116] also used flash X-ray radiation and studied the effect on both p-channel and n-channel silicon MOS thin-film transistors on a sapphire substrate. They noted that such devices were easier to analyze because they have a lower level of isolation junction photocurrent.

Ionization in Gas Discharge. Estrup[44,45] has used a gas discharge to create both positive and negative ions which he used in a variety of ways to study the surface effects of gaseous ions and electrons on semiconductor devices.

Conclusion

This body of literature provides the background to support a better understanding of the present status of planar device technology as a basis for further experimental work and for predicting technologies which are likely to result in improved devices.

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APPENDIX B

DEVICE EVALUATION DATA

Summary of Charge Densities in MOS Capacitors on n-Type and p-Type Si

Table B-1 is a summary of the measured charge densities found in MOS capacitors prepared on phosphorus doped silicon. Table B-2 is similar to Table B-1 except that the silicon involved is boron doped instead of phosphorus doped.

The silicon wafers were all cleaned with the same sequence of cleaning steps using both organic and inorganic solvents. The final step in the silicon surface preparation was either an etch in an acid solution containing HF, HNO_3 and HAc followed by a 1-minute rinse in DI H_2O, or it was a deposition of a fresh layer of epitaxial silicon.

The temperature at which the oxide, or nitride, layer was formed is given. The rinse or etch of the oxide preparatory to the metalization is shown. These pre-metalization treatments were either:

1. None,
2. Five seconds in 10:1 H_2O:HF followed by a 1-minute rinse in H_2O (deionized H_2O in all cases),
3. Five seconds in buffered HF (2 parts NH_4F, 1 part HF, 3 parts H_2O) followed by a 1-minute rinse in H_2O,
4. Thirty seconds in H_2O, or
5. One minute in methanol.

Each sample was alloyed in dry N_2 at 475° C for five minutes except as otherwise noted in Table B-1. Other variations also are noted in Table B-1.

All the charge densities were calculated as described in subsection 2.6 of the body of this report.

The symbol L in Tables B-1 and B-2 means that the measured mobile ion density was less than 10^{10} cm^{-2}. The symbol T means there was more trapping instability than mobile ion instability.

Threshold Voltages and Mobile Charge Densities of Transistors

Table B-3 shows the threshold voltages and mobile charge densities that we measured in transistors that were fabricated to establish feasibility that the improvements achieved in capacitor structures are compatible with transistor fabrication processes. The symbols L and T have the same meanings as stated above for Tables B-1 and B-2.

Influence of Transistor Processing Steps on the Mobile Ion Density

Table B-4 shows the results of an experiment to determine the source of mobile charge that was found in the first groups of transistors that were made to establish that transistors can be made with the improvements found in the experiments with capacitors. The variables are those that are involved in the fabrication of transistors but not in the fabrication of capacitors.

Results of an Experiment to Determine the Effects of Alloying, the Dryness of the Oxide, and the Temperatures Used in Mounting

Table B-5 shows the results of a series of experiments designed to show the effects of the alloying process (475°C, dry N_2, 5 min), the relative dryness of the oxide, and of the temperatures used in mounting and packaging on the densities of immobile charge, alkali ions and RT ions in MOS capacitors.

The oxides were thermally grown in dry O_2 at 1200°C to a thickness of 2000 Å. The dry oxides were cooled at and removed through the gas outlet end of the oxidation chamber. The very dry oxides were cooled at and removed through the gas inlet end of the oxidation chamber.

The difference between plain and gold refers to whether the bottom of the silicon wafer was coated with evaporated gold. Those devices that had the evaporated gold layer were mounted at lower temperatures. The plain chips were chip bonded at 400°C and wire bonded at 300°C. Chips with gold were chip bonded at 340°C and wire bonded at 25°C. This reduction in temperature for wire bonding was possible because an ultrasonic bonder was used.

The difference between wax and no wax refers to whether Apiezon wax was used to protect the top of the wafer while the oxide was etched from the bottom.

This data shows the reduction in immobile charge density that we routinely find for heat treatments at lower temperatures; i.e., the devices that were alloyed have lower immobile charge densities, and those (plain) devices that were mounted at the higher temperature have the lower immobile charge density. The densities of alkali ions or RT ions were not clearly influenced by any of the variables in this experiment.

Effects of Variables at Metalization

Table B-6 shows the results of experiments to show the effects of variables associated with the metalization and pre-metalization treatment of the oxide.

TABLE B-1

SUMMARY OF THE EXPERIM

ON n-TYPE MATERIAL, PHOS

	Sample Number	Silicon Surface Preparation	Insulator Formation Temperature	Pre-Metalization Preparation	Resistiv of Silic Orientat
	1A	EP	1200°C	None	4.0Ω-cm<
	119	Liquid	1200	None	3.1Ω-cm<
	119	Liquid	1200	None	3.1Ω-cm<
	119	Liquid	1200	None	3.1Ω-cm<
	122	Liquid	1200	None	3 1Ω-cm<
	122	Liquid	1200	None	3.1Ω-cm<
	123	Liquid	1200	None	22Ω-cm <
	125	Liquid	1200	None	19Ω-cm <
	144	Liquid	1200	None	4.9Ω-cm<
Thermally	148A	Liquid	1200	None	5.4Ω-cm<
Formed	151	Liquid	1000	None	4.5Ω-cm<
SiO_2	153	Liquid	1200	10:1 H_2O:HF	3.5Ω-cm<
	163	Liquid	900	Buffered HF	4.0Ω-cm<
	176B	Liquid	1200	None	2.8Ω-cm<
	177A	Liquid	1200	10:1 H_2O:HF	2.4Ω-cm<
	178A-152	Liquid	1200	None	3.0-4.0<
	178B	Liquid	1200	Buffered HF	3.1Ω-cm<
	179B	Liquid	1200	30_s DI H_2O	2.9Ω-cm<
	184A	Liquid	1200	30_s DI H_2O	4.0Ω-cm<
	184B	Liquid	1200	10:1 H_2O:HF	4.0Ω-cm<
	185A	Liquid	1200	10:1 H_2O:HF	4.0Ω-cm<
	185B	Liquid	1200	Methanol	3.0Ω-cm<
	161B	Liquid	1200	Buffered HF	3.1Ω-cm<
	229-230	Liquid	1200	Buffered HF	5.0Ω-cm<
	4A-6A	EP	1050	None	1.9Ω-cm
	187	EP	1050	Buffered HF	1.5Ω-cm
CO_2 Vapor	188	EP	1050	Buffered HF	1.0Ω-cm
Plated	190	Liquid	1050	Buffered HF	3.0Ω-cm<
SiO_2	8A	EP	1050	None	2.4Ω-cm<
	150	Liquid	1050	None	1.6Ω-cm<
	155	Liquid	1175	Buffered HF	1.0Ω-cm<
	165	Liquid	1050	Buffered HF	5.4Ω-cm<
SiH_4 Vapor	172	Liquid	1050	Buffered HF	1.0Ω-cm<
Plated	175	Liquid	830	Buffered HF	4.3Ω-cm<
SiO_2	182	Liquid	1270	Buffered HF	5.4Ω-cm<
	10A	EP	830	None	2.0Ω-cm<
Vapor Plated	189	Liquid	940	Buffered HF	5.0Ω-cm<
Si_3N_4	192	Liquid	940	Buffered HF	5.0Ω-cm<

Note #1 Alloyed at 550°C, 5 minutes.
Note #2 Alloyed at 475°C, 5 minutes.
Note #3 Not alloyed.
Note #4 Alloyed 475°C, 5 min., 1% dry N_2, 99% dry O_2.
Note #5 Ni treatment of impurities in Si after oxidation.
Note #6 99.99% pure CO_2.

NTAL DATA

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.ty on & .on	Miscellaneous Information	Charge Density ($\times 10^{-11}$) cm^{-2} Immobile	Alkali	RT Ions	Trapped
.11>		2.3-2.4	0.7	T	0.1
.11>	(See Note #1)	2.4-2.9	2.0	0.8	
.11>	(See Note #2)	3.1-3.2	0.5	0.2	
.11>	(See Note #3)	2.7-3.1	0.2	L	
.11>	(See Note #1)	2.7-2.8	1.0	L	
.11>	(See Note #3)	3.7-3.9	L	L	
.00>		0.4	0.3	L	
.11>	(See Note #4)	3.6-3.9	0.6	0.1	
.11>		2.0-2.2	0.8	0.4	
.11>	(See Note #5)	1.4-1.6	1.0	T	0.2
.11>		1.3-1.5	0.2	T	0.4
.11>		2.1-2.2	L	L	
.11>		1.9-2.2	0.1	L	
.11>		2.4-2.6	0.1	0.1	
.11>		2.0-2.1	1.2	0.3	
cm<111>		2.2-2.5	0.1	L	
.11>		2.1-2.2	3.0	1.2	
.11>		2.4-2.8	0.1	T	0.1
.11>		2.1-2.3	0.5	1.3	
.11>		1.8-2.3	0.7	0.6	
.11>		1.9-2.2	0.8	0.3	
.11>		1.9-2.5	3.7	2.1	
.11>	(See Note #9)	2.0-2.3	0.7	0.7	
.11>	(See Note #5)	0.5-1.2	1.2	0.4	
.11>	(See Note #6)	0.9-1.4	T	T	0.1
.00>	(See Note #6)	(-)0.3-<0.1	0.4	L	
.11>	(See Note #6)	1.2-1.4	0.1	T	0.2
.11>	(See Note #7)	2.7-3.2	T	T	0.4
.11>	(See Note #1&8)	1.0-1.5	0.4	7.0	
.11>	(See Note # 8)	1.5-1.7	0.3	T	0.2
.11>	(See Note #8)	1.2	0.8	T	0.2
.11>		1.9-2.4	3.0	T	1.9
.11>		3.1-3.5	1.6	T	0.3
.11>		3.9-10	1.5	0.9	
00>		10-13	8.0	T	2.0
.11>		14-15	T	T	0.6
.11>	(See Note #10)	24-27	T	T	6.0
.11>	(See Note #11)	24-26	T	T	5.0

Note #7 99.99% pure CO_2, P doped $SiCl_4$ used in making oxide.
Note #8 99.995% pure CO_2.
Note #9 75 min. DI H_2O substituted for 5 min. DI H_2O rinse in Si surface preparation procedure.
Note #10 Heated at 330°C for 2 hrs. after normal cooling process.
Note #11 Slow cooling: (1) 800°C for 10 minutes (2) 700°C for 10 minutes

TABL

SUMMARY OF THE

ON p-TYPE MATER

	Sample Number	Silicon Surface Preparation	Insulator Formation Temperature	Pre-Metalization Preparation
Thermally Formed SiO_2	231	Liquid	1200°C	Buffered HF
	232	Liquid	1200	Buffered HF
	233	Liquid	1200	Buffered HF
	234	Liquid	1200	Buffered HF
	235	Liquid	1200	Buffered HF
	236	Liquid	1200	Buffered HF

XPERIMENTAL DATA

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Resistivity of Silicon & Orientation	Miscellaneous Information	Charge Density ($x10^{-11}$) cm^{-2}			
		Immobile	Alkali	RT Ions	Trapped
14Ω-cm⟨100⟩		2.9-3.0	T	T	0.3
12Ω-cm⟨100⟩		2.7	L	0.3	
14Ω-cm⟨110⟩		3.6-3.7	T	T	0.4
14Ω-cm⟨110⟩		3.6-3.8	0.4	0.1	
14Ω-cm⟨111⟩		2.1-2.2	0.1	0.2	
16Ω-cm⟨111⟩		2.0-2.3	0.2	0.2	

TABLE B-3

THRESHOLD VOLTAGES AND MOBILE CHARGE DENSITIES OF p-CHANNEL MOS TRANSISTORS

	Unit Number	Threshold Voltage @ 20 μA	Alkali Ion Density ($\times 10^{-11}$ cm^{-2})	RT Ion Density ($\times 10^{-11}$ cm^{-2})	Trapped Charge Density ($\times 10^{-11}$ cm^{-2})
Group 210	1	0.3 V	0.25	0.05	--
	3	1.0	0.12	0.03	--
	9	0.6	0.25	0.05	--
	13	1.7	0.21	T	0.05
	20	1.6	0.15	T	0.06
	21	1.8	0.15	T	0.06
	23	1.4	0.46	T	0.08
	25	1.2	0.24	T	0.14
	Average	1.2	0.23	T	0.04
Group 213	1	1.8 V	1.10	0.11	--
	3	2.1	0.55	0.06	--
	2	1.4	2.4	0.3	--
	4	2.3	0.96	0.15	--
	5	1.8	0.80	0.08	--
	6	1.3	0.55	0.05	--
	7	1.6	1.34	0.03	--
	9	2.6	1.29	L	--
	10	2.4	0.46	L	--
	11	1.8	1.52	0.03	--
	12	1.9	1.06	L	--
	13	2.4	1.34	0.03	--
	22	2.4	0.70	T	0.03
	Average	2.0	1.08	0.07	--
Group 217	1	5.9 V	T	T	0.23
	3	5.6	T	T	0.55
	7	6.0	0.38	L	--
	8	5.7	T	T	0.15
	9	5.5	T	T	0.56
	10	5.7	0.03	T	0.15
	12	5.7	0.70	L	--
	16	5.8	0.61	T	0.08
	17	6.2	0.91	L	--
	19	5.9	0.46	T	0.11
	22	6.4	0.91	T	0.05
	Average	5.9	0.57	L	0.17

NOTES:

Group 210

Thermally grown oxide on Sb doped, 6.7 Ω-cm, ⟨100⟩ silicon.

Group 213

Thermally grown oxide on Sb doped, 6.3 Ω-cm, ⟨100⟩ silicon.

Group 217

Thermally grown oxide on P doped, 1.5 Ω-cm, ⟨111⟩ silicon.

TABLE B-4

INFLUENCE OF PROCESSING STEPS INVOLVED IN FABRICATING TRANSISTORS

	Charge Density ($\times 10^{-11}$)		
	Immobile	Alkali	RT Ions
Oxidation in dry O_2	1.8-2.3 cm^{-2}	1.1 cm^{-2}	0.4 cm^{-2}
Oxidation in dry O_2 plus diffusion (boron)	1.5-2.0 1.4-1.9	2.0 2.1	0.7 0.3
Oxidation in dry O_2 plus photolith steps	1.8-2.0	0.2	0.1
Dry-wet-dry oxidation	1.7-2.0	1.3	0.1
Dry-wet-dry oxidation plus diffusion (boron)	1.3-1.5 1.4-1.9	2.0 3.4	0.4 0.8
Dry-wet-dry oxidation plus photolith steps	1.8-2.3	1.6	<0.1

TABLE B-5

COMPARATIVE DATA SHOWING THE EFFECTS OF ALLOYING, MOISTURE CONTENT, AND TEMPERATURES INVOLVED IN PACKAGING DEVICES, n-TYPE Si. ALL VALUES ARE CHARGES PER cm^2 DIVIDED BY 10^{11}

n-TYPE MATERIAL	ALLOYED 475° C, 5 MIN.				NOT ALLOYED			
	D R Y		V E R Y D R Y		D R Y		V E R Y D R Y	
	PLAIN	GOLD	PLAIN	GOLD	PLAIN	GOLD	PLAIN	GOLD
IMMOBILE CHARGE								
WAX	1.5-1.8	1.8-1.9	2.2-2.4	2.1-2.3	2.1-2.3	2.9-3.1	2.5-3.0	4.5-4.7
NO WAX	1.5-1.8	1.7-1.9	2.0-2.5	2.0-2.3	1.9-2.1	2.6-2.8	2.4-2.9	2.9-3.6
ALKALI IONS								
WAX	1.7	1.7	0.8	1.3	2.0	0.2	2.7	-0.9*
NO WAX	1.5	2.6	0.7	1.3	2.7	1.6	2.5	0.1
RT IONS								
WAX	0.6	0.5	0.2	0.5	0.1	0.4	1.7	-0.1*
NO WAX	0.2	1.2	0.2	0.4	1.1	1.1	1.3	0.1

* Trapping.

Note: For explanation of the difference between PLAIN and GOLD see the last paragraph on page B-2.

TABLE B-6

EFFECTS OF VARIABLES ASSOCIATED WITH THE METALIZATION AND PRE-METALIZATION TREATMENT OF THE OXIDE

Sample #	Oxide Etch and/or rinse	Metalization Conditions	Alkali Ions	RT Ions
176B	None	U, E, 5×10^{-8}	0.1×10^{11} cm^{-2}	0.1×10^{11} cm^{-2}
177A	10:1 HF, 5 sec.	U, E, 10^{-6} Torr	1.2	0.3
177B	10:1 HF, 5 sec.	U, E, 5×10^{-8} Torr	1.8	<0.1
178B	BHF, 5 sec.	U, E, 5×10^{-8} Torr	3.0	1.2
178A	None	U, E, 10^{-6} Torr	0.1	<0.1
179B	DI H_2O, 30 Sec.	U, E, 10^{-6} Torr	0.05	-0.1*
179A	DI H_2O 30 Sec.	Production Metalizer	16.8	3.7
176A	None	Production Metalizer	32.2	3.5

- - - - - - - - -

* Trapping

U Ultek Vacuum System

E Electron Gun Evaporator

The production metalizer is a CVC vacuum system with a tungsten coil evaporator.

APPENDIX C

DEVICE STRUCTURAL DATA

The capacitors described in this report were made with evaporated aluminum which was photolithographically delineated into circular electrodes of either 20- or 36-mil diameter.

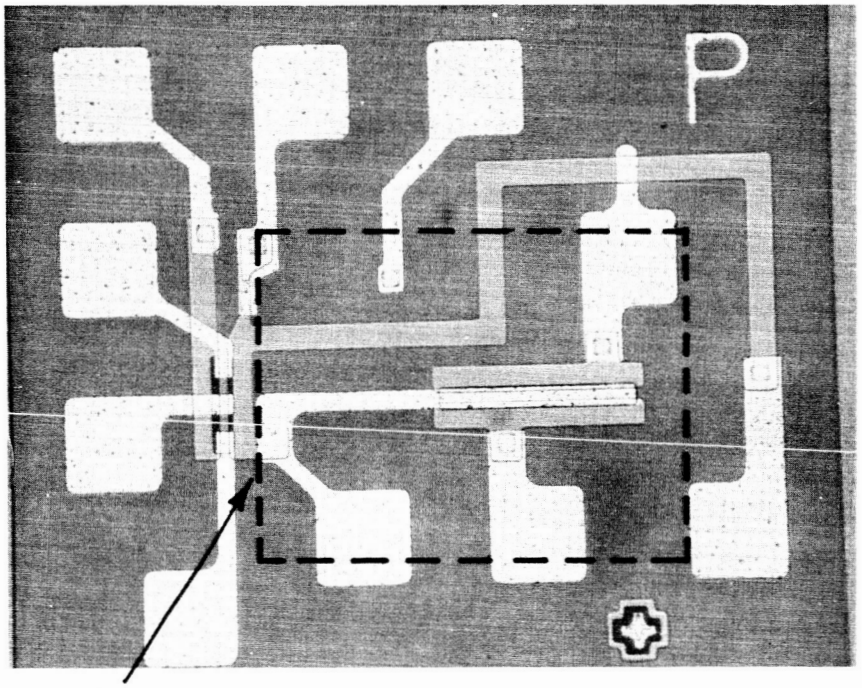
The transistors were formed in a microcircuit pattern as shown in Figure C-1. Figure C-2 shows the transistor structure on which our measurements were taken. Other structural data for these transistors is given in Table C-1.

M = 131X

Thermally grown gate oxide

Gate width = 8 mils

Gate metal thickness = 1 mil



See Figure C-2 for enlarged view

Figure C-1. Microcircuit configuration in which transistors were made for evaluation.

M = 264X

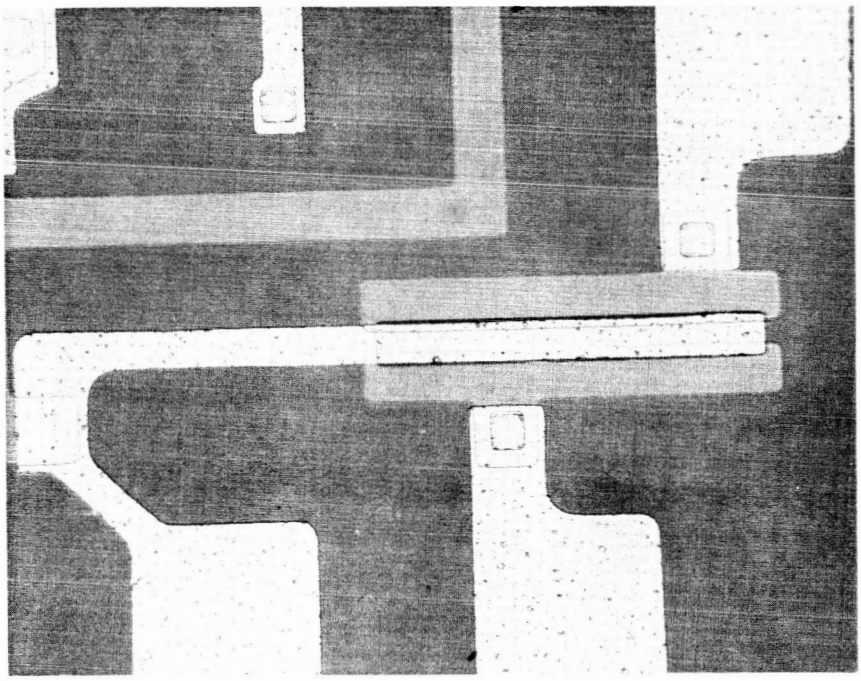


Figure C-2. Structure of the transistors which were evaluated.

TABLE C-1

TRANSISTOR STRUCTURAL DATA

GROUP NO.	ORIENTATION	PREPARATION OF GATE OXIDE	GATE SiO_2 THICKNESS	GATE WIDTH	DIFFUSION LAYER DEPTH, X_J	FINAL GATE LENGTH (see Note 1)	CHANNEL WIDTH TO LENGTH RATIO, W/L
210	⟨100⟩	Thermally grown	1400-1500Å	8.0 mils	0.18 mils	0.23 mils	34
213	⟨100⟩	Thermally grown	1400-1500Å	" "	" "	" "	34
215	⟨111⟩	Thermally grown	1400-1500Å	" "	" "	" "	34
217	⟨111⟩	Thermally grown	1400-1500Å	" "	" "	" "	34
226	⟨100⟩	Vapor deposited	1600-1800Å	" "	0.12 mils	0.32 mils	25
227	⟨111⟩	Vapor deposited	1300-1450Å	" "	" "	" "	25

Note 1: In calculating the final gate length, the lateral diffusion distance under the gate was assumed to be 75% of X_J.

APPENDIX D

RELEVANT INFORMATION FROM THE FIELD OF GLASS TECHNOLOGY

Introduction

To bring to the program the benefits of the fundamental and empirical knowledge available in the field of glass technology, Professor A. E. Owen of the Department of Glass Technology, University of Sheffield, Sheffield, England, was retained as a consultant. Professor Owen's extensive knowledge in the field of the electrical properties of glass and vitreous silica is evident in two of his papers: "Electrical Conduction and Dielectric Relaxation in Glass," Progress in Ceramic Science, 3, 77-196 (1963); and "The Electrical Properties of Vitreous Silica," co-authored with R. W. Douglas, J. Soc. Glass Technology, 43, 159T-178T (1959).

Professor Owen was informed of the objectives of this program before he attended the Silicon Interface Specialists Conference in Las Vegas, Nevada, November 15-16, 1965. Philco personnel were active in organizing and participating in this conference, which was sponsored by the Electron Devices Group of IEEE. It brought together approximately 85 specialists active in the field of MOS

physics and technology. The objective was to bring about a free interchange of ideas to increase the knowledge and understanding of silicon interface phenomena. An effort was made to include representatives of all known research laboratories and manufacturers active in the field of MOS devices in the United States.

At this conference, Professor Owen became conversant with the state-of-the-art in MOS technology and the chief problem areas. After the conference, he visited the Advanced Development Laboratory of Philco's Lansdale Division for consultation. On December 17, 1965, having had time to consider the problems, he prepared the following report.

Professor Owen's Report

What contribution can glass science and technology make to the problems of instability in MOS devices which are caused by the motion of charges in the SiO_2 layer? The first reaction of a glass specialist to this question must be to ask, "Are SiO_2 films grown thermally on silicon at relatively low temperatures really 'glasslike'?"

Glasses are essentially supercooled liquids with a continuous (continuous in the normal silicate glasses; glasses with discontinuous networks are known) frozen-in network having a non-equilibrium liquid-like configuration. The exact configuration depends very much on the rate of cooling from the liquid; as a consequence the two features characteristic of the glassy state are(1):

1) The existence of a transformation range; i.e., a temperature interval in which the frozen-in glassy configuration can, within experimental times, relax to take up the equilibrium configuration and hence give rise to time-dependent properties in this temperature range.
2) The physical (and chemical) properties are sensitive to thermal history. The position of the transformation range itself depends upon

the cooling rate, becoming lower in temperature the slower the rate. This sensitivity to thermal history is, however, no more than a consequence of the existence of the transformation range phenomenon (1).

There are cases where the films grown on silicon are, at least in part, glassy -- e.g., after treatment in P_2O_5 vapor at high temperature during which a liquid layer is probably formed. In general, however, to correctly describe SiO_2 films grown on silicon as glasses -- and hence to draw on what is known about the glassy state -- it would strictly be necessary to demonstrate the existence of a transformation range in the SiO_2 films. To carry out an experiment to elucidate this point would probably be very difficult. It is true that MOS device characteristics are sensitive to heat treatment processes, but to what extent this is due to "relaxational changes in the bulk" of the oxide film rather than effects at the interfaces or even in the silicon itself, is not clear, and to separate the various sources of change in such a complex system would also be a difficult task.

In raising this question one is not being merely pedantic, for the effects of transformation range phenomena on the physical properties of glasses at room temperature are not trivial. Take,

as an example, the electrical resistivity -- probably the most relevant property in the present context. The room temperature resistivity of a typical soda-lime-silicate glass can vary by an order of magnitude between a rapidly chilled and a well-annealed specimen; compositionally, this change in resistivity is equivalent to a very considerable difference in the sodium concentration. Obviously such effects cannot be overlooked in interpreting the physical properties of glasses.

What, therefore, is the nature of SiO_2 films grown on silicon? No doubt they are amorphous, but could they be very finely divided polycrystalline layers? If this were the case, grain boundaries would of course be very important in diffusion mechanisms, and comparisons with glass or bulk crystalline forms of silica would be quite invalid. The good strength, hardness and scratch resistance of the films perhaps argues against this but is not conclusive. The most direct test would be low-angle X-ray diffraction, for a glass should not show low-angle scatter (cf. with silica gel). Alternatively, one should ask whether there is any anisotropy in the SiO_2 films. Is there, for instance, a preferred orientation perpendicular to the silicon surface; e.g., a configuration corresponding to the c-axis of quartz?

To reiterate: The essence of glass formation is a continuous change in energy, entropy and volume on going from the liquid to the glassy state, but with discontinuities in derivative properties [1]. It is difficult to conceive that there can be a similar continuity between the phases involved in the formation of thermally grown SiO_2 films on silicon, and in this sense these films cannot be "glassy". To what extent this difference in "thermodynamics" affects the properties is problematical, and subsequently the assumption is made that meaningful comparisons between glasses and the SiO_2 films in MOS devices <u>can</u> be made. One is encouraged in this assumption by the fact that the SiO_2 films have dielectric properties, an index of refraction and a density comparable to those of fused silica; there are twenty-two phases of silica, and at least some of these are likely to have properties not very different from fused silica.

Before proceeding, one more note of caution should be sounded. The great majority of electrical measurements on glasses have been made in the low-field condition, i.e., less than 10^3 V/cm, where Ohm's law applies. This contrasts with the much higher field strengths normally involved in MOS device studies. Generally, however, glass continues to be an electrolytic (cationic) conductor

at high field strengths and the same type of ionic model may be applied to the high field conductivity [2]. This is probably true even at breakdown which normally occurs by Joule heating and thermal catastrophe, rather than by electron avalanche.

The critical property of the SiO_2 in MOS structures is its ability to store and transfer charge, and it has been proposed by several authors that the charged species responsible for the electrical properties of the oxide is an oxygen vacancy (V^{++}) [3]. If, however, there is any similarity to the conduction mechanism in bulk glass, this would seem unlikely. This is not to say that oxygen vacancies do not exist in glass; a model based on oxygen deficiency has been proposed for certain paramagnetic centres in glass observed by electron-spin-resonance experiments after neutron irradiation [4]. It is a fact, however, that oxygen ion diffusion in glasses is very small indeed, and many orders of magnitude less than for common cations such as the alkali ions. Because of this large difference it is not easy to compare oxygen and sodium ion diffusion coefficients at the same temperature, but where this is possible (e.g. at 450°C) experimental results indicate that the diffusion coefficient for oxygen is at least a factor of 10^7 lower than that for sodium ions [5]; at room

temperature the difference is likely to be even greater. The diffusion coefficients and (electrical) mobility are directly related to each other through the Nernst-Einstein equation [2] so that if oxygen ion vacancies are to make an equal contribution to the conductivity, and hence charge transfer, they would have to be in a concentration at least 10^7 times greater than the sodium ions. Sodium is one of the most troublesome of impurities and it certainly seems likely that in fused silica the conductivity can be attributed to contamination by sodium or other alkali ions [6]. This is apparently so even in the purest grade of fused silica -- the synthetic varieties produced from semiconductor quality silicon via a volatile halide -- which contains only a few parts of alkali per hundred million, i.e. approximately 10^{14} per cc. In the normal commercial grade of fused silica - produced from natural quartz - the alkali impurity level is measured in parts per million.

The opportunities for contamination of the oxide in MOS structures are such (e.g. during oxidation by transport from the reaction tube or from the gases themselves, during etching or photoresist treatments, etc.) that it would be surprising if sufficient sodium or other alkali were not present in sufficient

quantities to have a dominating effect on the electrical properties of the oxide film. At the IEEE Silicon Interface Specialists Conference in Las Vegas, November 15-16, 1965, levels of 10^{15} Na atoms/cc seemed to be regarded as the best obtainable purity under present conditions, and most oxide films probably have more. By comparison with the situation in fused silica this would, in the writer's opinion, be enough for the sodium impurity to effectively control the conduction mechanism in the oxide. If, in these circumstances, oxygen ion vacancies were sufficiently mobile to carry an appreciable part of the current this would in itself suggest a significant difference between the oxide film in MOS structures and fused silica and glasses. It should be pointed out, however, that if there was a relatively large concentration of oxygen ion vacancies capable of limited movement, these could contribute to charge motion by dielectric polarization. The sodium ions will also contribute to polarization, of course, by dielectric relaxation [2]. In addition, it must be remembered that in "wet" grown oxides there will probably be relatively large amounts of protons which might be expected to be even more mobile than alkali ions. This situation is slightly more complicated,

however, because the protons are associated with hydroxyl groups and the work of Hetherington, et al have shown that in glasses there are mobile and immobile forms of the hydroxyl group [7-9].

If, therefore, comparisons with glasses are valid one can conclude that the predominant mechanism of charge transfer in the oxide of the MOS structure is by sodium and/or hydrogen ion migration. Moreoever, it is unlikely, because of the various treatments used, that the sodium contamination could be reduced to a level where it is insignificant in this respect. Electrolysis would perhaps remove all or part of the sodium ions or protons, but for the electrolysis to proceed to any extent the ions removed would have to be replaced by some other species of comparable mobility. The electrochemistry could be quite complex, but in the simplest terms, if the silicon was made positive and the metal negative, sodium would only be removed if:

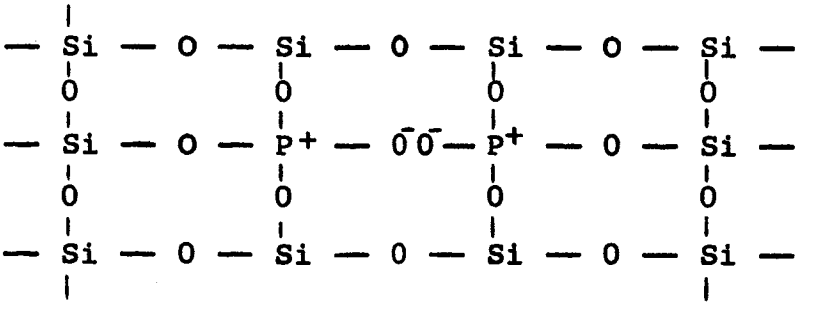
1) Positive "holes" (presumably oxygen ion vacancies) entered at the silicon-oxide interface, and

2) The sodium ions could be discharged at the metal.

If the positive "holes" were not reasonably mobile, charge separation would occur, setting up an opposing space-charge, and the electrolysis current might drop to negligible proportions.

A similar effect would occur if the metal electrode did not discharge the sodium ions.

Supposing, however, electrolysis could be achieved in the manner postulated, the sodium ions would have been replaced by an equivalent amount of positive oxygen ion vacancies. It might be possible to remove these by a subsequent oxidation or high temperature treatment, but even this presents difficulties (see later paragraph). Failing in the effort to eliminate or remove the alkali impurity, the only other alternative is to reduce its mobility by some means. This would seem to be the function of treatments in P_2O_5 vapor which are reported to improve the stability of MOS structures [10]. Phosphorus can replace the silicon in SiO_2 isomorphously and when introduced in the form of P_2O_5 may cause the formation of non-bridging oxygen ions and $P^+ - O^-$ dipoles:



The effect of P_2O_5 in SiO_2 may be twofold:

1) The dipoles may act as "traps" for the alkali ions, hence reducing their mobility (N.B., the ion-dipole interaction is relatively strong).
2) By forming non-bridging oxygens the P_2O_5 may break down the continuous glassy network. This effect might increase the mobility of modifying ions.

Insofar as theory has progressed, it appears that the barrier to ionic motion in glasses is predominantly electrostatic rather than spatial or configurational (see Ref. 2 pp 121-122 and pp 180-184); the first effect would probably be the most important, therefore, leading to an over-all decrease in mobility of the alkali ions. In circumstances where the alkali is in trace amounts with relatively large concentrations of P_2O_5, this conclusion seems even more likely.

Alternatively, an even simpler explanation could be postulated in purely "chemical" terms; namely, the phosphate glass may be expected to have a greater affinity for the alkali (because P_2O_5 is a more electronegative oxide than SiO_2), so that an outer layer of phosphate glass would act as a "getter" for alkalis. This chemical approach may be given added weight by the observation

that treatment with B_2O_3, unlike treatment with P_2O_5, tends to degrade the stability of MOS structures. On the "physical" arguments used above this is surprising, for B_2O_3 is known (a) to decrease the conductivity of sodium silicate glasses [2], and (b) to make the glass more compact (provided not too much B_2O_3 is added), i.e., to increase the density. On the other hand this would be consistent with the chemical argument for B_2O_3 is less electronegative than SiO_2 and alkalis would therefore tend to favor the latter. This is not a very conclusive observation, however, because it is extremely difficult to obtain B_2O_3 completely free of water, and it is possible that in the B_2O_3 treatment appreciable amounts of water (protons) will enter the oxide layer.

Phosphorus and boron are network-forming oxides. The other method of reducing the mobility of alkali ions in silica would be to introduce larger and relatively immobile network modifying oxides. For example, barium oxide is known to increase the resistivity of a sodium silicate glass by three orders of magnitude when the BaO is substituted for SiO_2 in an equivalent amount to that of the Na_2O [2]. If the barium was present in excess, a larger effect might be expected. The oxides of calcium, strontium and lead also increase the resistivity appreciably, but to a smaller extent than barium.

The resistivity of glasses is also increased considerably by the "mixed alkali effect" [2]. Glasses containing either Na_2O or Li_2O, say, in equivalent amounts, have roughly the same resistivity, but if Na_2O is substituted for some of the Li_2O in the glass the resistivity does not change linearly but goes through a very pronounced maximum when the Na_2O and Li_2O are present in roughly equimolecular amounts. The resistivity of the mixed alkali glass may be four decades higher than either of the single alkali glasses. The effect is found for any pair of alkalis and may be more pronounced the greater the size difference between the two alkali metals. At the present time there is no satisfactory explanation for this phenomenon but the most plausible one is based upon the idea that during glass formation each alkali ion tends to influence its own environment and to create "holes" which are energetically favorable to itself [2]. During subsequent migration, therefore, the larger ion sooner or later finds itself confronted by a "hole" vacated by a smaller ion, its motion is blocked, and hence all ionic migration stops. In its simplest terms this explanation does, in fact, lead to a zero conductivity (see Ref. 2 pp 136-139).

It is conceivable that one might make use of either the "heavy ion" or the "mixed alkali" effects to reduce the alkali

ion mobility in the MOS structure. But the nature of glass and the glass-forming process should again be borne in mind and contrasted with the processes involved in forming MOS devices. Glasses are formed from a melt and network-modifying ions (alkalis or alkaline earths) in the melt have the opportunity, during the cooling process, of influencing their own environment to a considerable extent, i.e., to "dig" holes which are energetically favorable. There is no reason to suppose that an ion introduced into a solid glass by diffusion, say, after cooling, would have exactly similar properties to the same type of ion melted into the glass. Since most of the alkali impurity in the MOS structure is probably introduced after the oxide formation, this is an important distinction. If, for instance, it was suspected that the impurity was mainly sodium and that this was introduced by contamination and diffusion from etching solutions, it would not be advisable to attempt at the same time to diffuse in a roughly equivalent amount of potassium, hoping to make use of the mixed alkali effect in reducing the sodium ion mobility. The net result would almost certainly be equivalent to having twice as much sodium present! Similarly, it would not even be advisable to deliberately introduce a larger alkali atom during growth, hoping that this would counteract the effect of sodium

introduced at a later stage by diffusion. The larger alkali ion, present on its own, would have a mobility not very different from sodium, and the sodium diffused in subsequently by contamination would not -- accepting the explanation mentioned above -- have the opportunity of inducing the mixed alkali effect. It would seem more profitable to try the inclusion of a large multivalent network-modifying ion which is known to have a low diffusion coefficient (e.g., BaO or PbO) but, again, this should be incorporated during the growth of the oxide.

All of the foregoing discussion has been concerned with reducing the mobility of the relatively mobile ions responsible for charge transfer. It is more difficult to make suggestions for the removal of "fixed" charges, i.e., those charges which exist independent of time or of treatment. It is accepted that the oxide layer grows by oxygen diffusion and the general concensus of opinion is, apparently, that this growth occurs by an ionic mechanism involving oxygen vacancies rather than by molecular or atomic diffusion of oxygen (although there seems to be some doubt about this in "wet" grown oxides). If this is the case, then there must always be a finite concentration gradient of positively-charged oxygen ion vacancies. In a free SiO_2 film

these could probably be virtually completely removed by an annealing treatment in an oxidizing atmosphere. But with an oxygen sink always present in the MOS structure (i.e., the silicon) an oxidizing treatment would presumably result simply in an increase in the thickness of the oxide, with perhaps a dilution of the non-stoichiometry, at best. By immobilizing the alkali ions, a considerable reduction in the dielectric polarization is likely to result. In glasses containing more than a few percent of alkali, for instance, the alkali ions not only cause the conductivity but also dominate the dielectric relaxation up to frequencies of at least 1 MHz and probably beyond [2]. In fused silica, however, water present in small amounts may control the dielectric properties [6].

An alternative may be to lay down films, instead of SiO_2, of a glass known to have good dielectric properties. Materials which come to mind are the boroaluminates, particularly those of calcium, strontium, barium, lead and bismuth, most of which have been studied in some detail. Attempts have been made to deposit rather complex glasses, e.g., lead or zinc aluminoborosilicates, and encouraging results have been obtained [11]. Generally, however, these glass films have been

deposited by inconvenient sedimentation techniques. A more convenient method, suited to continuous processing, might be to first evaporate a comparatively thick aluminum film onto the silicon and then to oxidize this in B_2O_3 vapor; the other metal (e.g., lead or zinc) could be introduced either by depositing it with the aluminum or by carrying it in the vapor phase with the B_2O_3. The oxidation should be continued until all of the aluminum, and probably some of the underlying silicon, has been oxidized.

Most of the boroaluminate glasses are known to have good electrical properties. The resistivity can be appreciably greater than that of the best quality of fused silica. The dielectric loss is small, changes only slowly with temperature up to 200 or 300°C and is only slightly dependent on frequency in this same temperature range. The dielectric constant is practically constant, indicating little dielectric polarization, for frequencies between 10^2 and 10^5 Hz in this temperature range. At room temperature the dielectric loss does not begin to increase sharply until frequencies higher than 10 MHz are reached. Variations on this method can be imagined for specific circumstances. The boroaluminates may, for instance, be sensitive

to atmosphere moisture. This depends on composition, but their inertness can be greatly improved, without detracting from the good electrical properties, by incorporating some silica. In the film formation technique this could be achieved by depositing silicon monoxide, say, along with the aluminum, or by oxidizing also some of the underlying silicon and raising the temperature to the point where the boraluminate glass is molten, thus eventually forming a boroaluminosilicate.

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